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Materials Development for Gallium Nitride Power Devices

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by

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Materials Development for Gallium Nitride Power Devices

This dissertation is dedicated to my parents, Meena and Mahesh Agarwal

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27. "Investigation of Mg δ-Doping for Low Resistance N-polar p-GaN Films Grown at Reduced Temperatures by MOCVD", Cory Lund, **Anchal Agarwal**, et al., Compound Semiconductor Week, Boston MA, 2018.

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34. "First report of scaling a normally-off In-Situ Oxide, GaN interlayer based vertical trench MOSFET (OG-FET)", Dong Ji, Chirag Gupta, **Anchal Agarwal** et al., Device Research Conference, South Bend, Indiana, 2017.

35. "Impact of threading dislocations on the device performance of GaN trench MOSFETs and potential yield of large area devices", Chirag Gupta, Silvia Chan, **Anchal Agarwal**, et al., International Symposium on Compound Semiconductors, Berlin, Germany, 2017.

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41. "Regrown Mg doped GaN interlayer to enhance breakdown voltage in trench MOSFET", Chirag Gupta, Yuuki Enatsu, Silvia H. Chan, **Anchal Agarwal**, et al., International Workshop on Nitrides, Orlando FL, 2016

42. "Comparison between GaN trench MOSFETs with $(11\bar{2}0)$ a-plane and $(10\bar{1}0)$ m-plane sidewalls", Chirag Gupta, Stacia Keller, Silvia H. Chan, Yuuki Enatsu, **Anchal Agarwal**, et al., Lester Eastman Conference, Bethlehem PA, 2016.

43. "MOCVD Based Amorphous (Al,Si)O Dielectrics for GaN MOS Capacitors: A Route to Improved Interface and Bulk Properties", Silvia H. Chan, Davide Bisi, Onur S. Koksaldi, Chirag Gupta, **Anchal Agarwal**, et al., Electronic Materials Conference, Newark DL, 2016.

ABSTRACT

Materials Development for Gallium Nitride Power Devices

by

Anchal Agarwal

Gallium Nitride has gained prominence in the field of power electronics due to its high bandgap, high critical electric field, high mobility and high saturation-drift velocity. This means that GaN can be used to make devices that have a low on-resistance along with a high breakdown voltage. High frequency GaN HEMTs have been commercially available since 2006 and still being improved. The high power market is just starting to tap into GaN devices. Vertical transistors are especially attractive for high power applications, as they provide the possibility of a high breakdown voltage at a low chip size, thus, a low cost price. In addition to this, GaN devices can also use the two-dimensional electron gas formed at the GaN/AlGaN heterojunction to obtain a higher current.

Several GaN based power devices are being investigated - both vertical and lateral. Our group has been focusing on the Oxide GaN-interlayer Field Effect Transistor (OGFET) and the Current Aperture Vertical Electron Transistor (CAVET). On the lateral side, power HEMTs are being developed. This work focuses on materials development for the various types of power devices. A primary motive for this thesis is for it to serve as a reference manual for researchers working on GaN power devices.

Vertical power devices are united by a common feature – a thick drift region with a low n-type carrier concentration. Through simulations, it has been shown that the optimal carrier concentration to simultaneously achieve a low R_{on} and a high breakdown voltage is about 1 x

10^{16} cm^{-3}. Through our experiments, it was demonstrated that it is also the carrier concentration range where the electron mobility peaks. Achieving such a low doping can be problematic as it is in the range of impurity dopants such as Carbon and Oxygen. A low doping and record mobility was achieved for vertical devices by MOCVD and applied to the OGFET and the CAVET. Devices were grown both, on sapphire and on bulk GaN and high breakdown voltages were achieved.

Power devices require an elaborate growth and fabrication process, including regrowth on p-GaN doped by Magnesium and regrowth within trenches. Magnesium is known to diffuse into subsequent layers during regrowth, lowering device performance. A novel approach to circumvent this issue is presented, which can eliminate the need to remove the sample from the MOCVD chamber altogether. A low temperature GaN layer grown via flow modulation epitaxy successfully suppressed the Mg penetration at a rate of 5 nm/dec, the lowest ever by MOCVD, leading to the formation of an abrupt p-GaN:Mg/GaN junction.

Regrowth within trenches was optimized for different applications. GaN was grown conformally within narrow trenches by exploring various growth conditions. A complete filling of trench was also achieved for a different set of applications. Finally, conformal regrowth of high composition, low temperature AlGaN was optimized for deep-recessed gate HEMTs to lower gate leakage. All of these were planar regrowths and no masks were used.

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1 Introduction

Energy consumption has increased by leaps and bounds since the industrial revolution, especially in the developed world.[1] Non-renewable energy sources - consisting of coal, oil, natural gas and uranium fuel - still form the bulk of the energy sources. It is estimated that more than 80% of energy consumed in the world still comes from fossil fuels, and this trend will continue till 2040. Unfortunately, the world has limited fossil fuel and nuclear energy sources, and it is becoming increasingly important to conserve energy. As of now, approximately 10% of all energy losses take place during conversion. Thus, even a slight improvement in power conversion efficiency can save significant amounts of non-renewable energy sources from getting wasted.

Modern computers, communication systems and electronic systems all require power electronic components at the interface of an electrical source and a load. The main task of power electronics is conversion – DC to AC, AC to DC, DC to DC and AC to AC. Examples of power conversion at various stages of power transmission is given in figure 1.1. Power conversion components can consist of simple circuitry, such as a half wave rectifier which uses a single diode, or have much more complex designs involving multiple stages and any number of transistors and diodes. Examples of the various types of converters include:

DC to AC: Inverters

AC to DC: Rectifiers

DC to DC (voltage level can be changed): Buck, boost and bridge converters

AC to AC (voltage and frequency can be changed): Cyclo, link and matrix converters

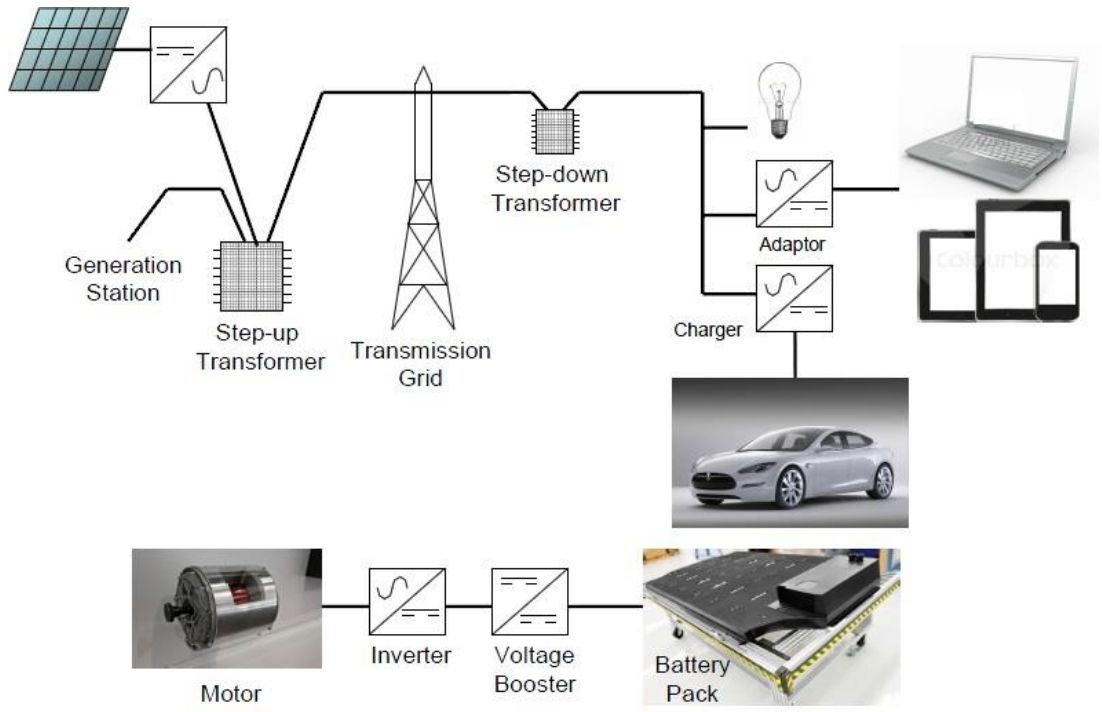

Figure 1.1: Power conversion from AC-DC, DC-AC, DC-DC and AC-AC takes place at various stages of energy transmission. Power electronic components are present in each stage of power conversion.

Power semiconductor devices form the core of power electronics and are commonly used as switches or amplifiers. An ideal switch has three primary requirements: a low on-resistance, high saturation currents, and a high breakdown voltage. It should be able to deliver any amount of current without a voltage drop or withstand high voltages without passing current. It is also highly desirable to have high switching frequencies. Figure 1.2 is a schematic of these metrics.

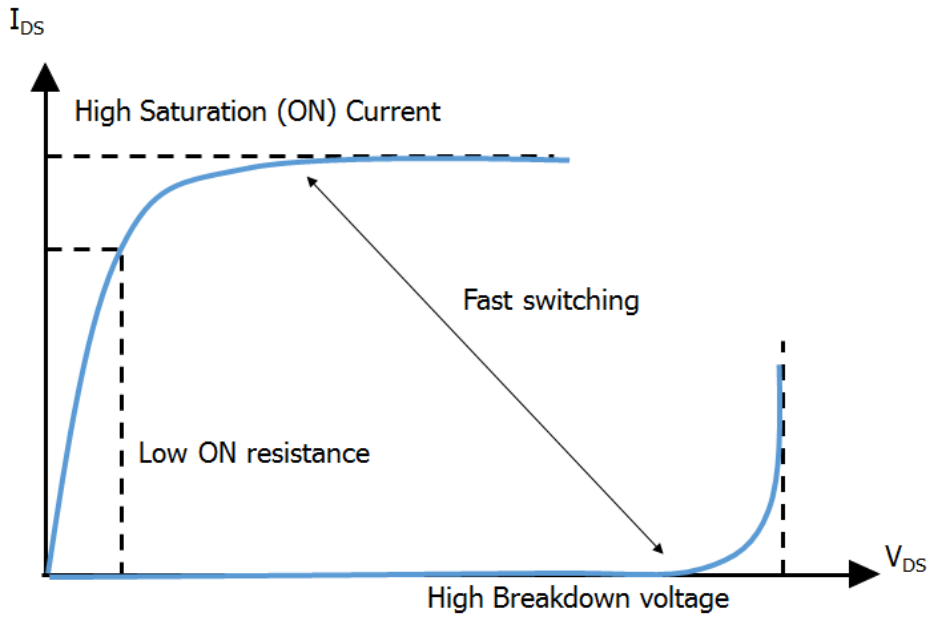

Figure 1.2: Desired characteristics of a power transistor – a high on saturation current (I_{ON}), low on resistance (R_{ON}) and a high breakdown voltage (V_{BR}).

Although Silicon (Si) is still most widely used in the industry, it is slowly reaching its fundamental material limits. There has been a growing interest in alternative semiconductors such as Gallium Nitride (GaN), Silicon Carbide (SiC) and Diamond. Gallium Oxide (Ga_2O_3) is an emerging semiconductor of interest as well, although still in its nascent stage. The fundamental property that binds these emerging power semiconductors is their wide bandgap, which translates to a high breakdown field, and a very high electron mobility. The defining equation for the absolute maximum power density is the figure of merit for power transistors and is given in the expression 1.1:

$$P = \frac{V_d^2}{R_{on}} = \mu E_{crit}^3 \varepsilon_s \qquad 1.1$$

The Baliga Figure of Merit (BFOM) is a more realistic estimate of the breakdown voltage, and is commonly used for power devices. The only difference is a factor of 4, as given in expression 1.2.

$$\text{Baliga FOM} = \frac{4.V_d{}^2}{R_{on}} = \mu E_{crit}{}^3 \varepsilon_s \qquad 1.2$$

Figure 1.3 shows the theoretical limits of the on-resistance vs. the breakdown voltage (or the Baliga FOM) of a device in a given material system. Table 1-1 compares the material properties of the main contenders for power electronics, including the theoretical limit for their respective power densities. GaN has a better FOM than its current competitors, SiC and Si, even though developing technologies such as diamond and β-Ga_2O_3 show tremendous potential.

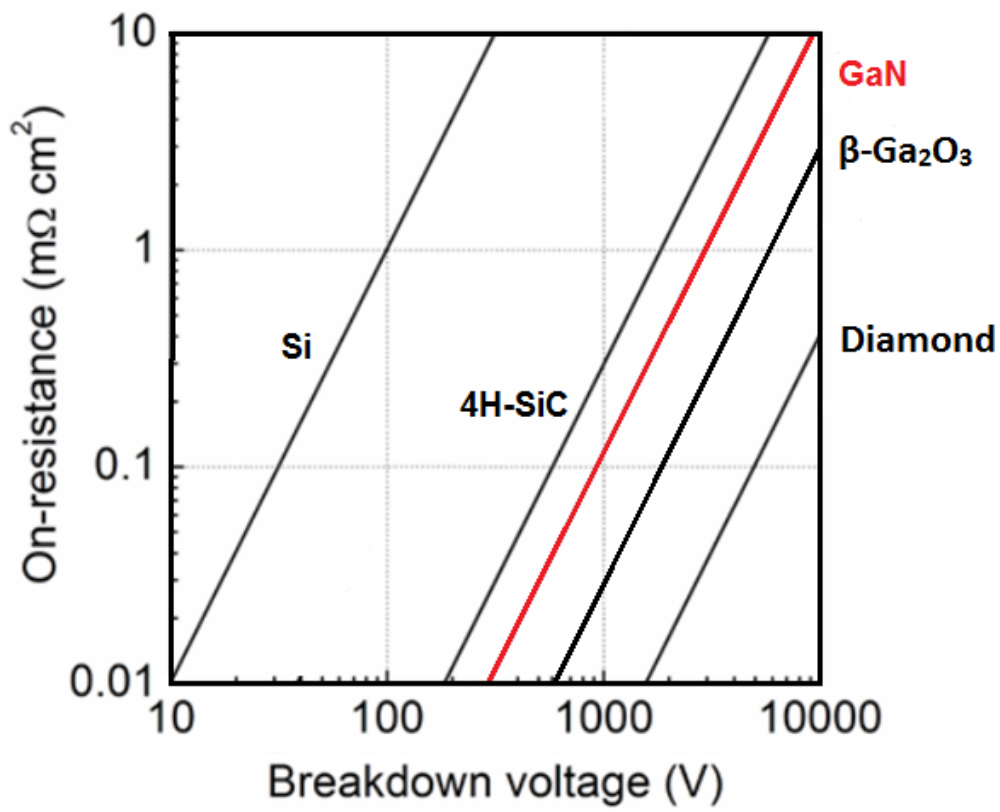

Figure 1.3: Theoretical limits of the BFOM of different power semiconductors.

Semiconductor Material	Si	GaN	SiC-4C	Ga_2O_3	Diamond
Relative Permittivity	11.7	8.9	9.7	10	5.7
Bandgap (eV)	1.1	3.4	3.2	4.8	5.5
Critical Electric Field (MV/cm)	0.3	3.3	2.5	8	10
Electron Mobility ($cm^2/V.s$)	1500	1200	1000	300	1800
Electron Saturation Velocity (10^6 cm/sec)	9	25	30	20	20
Thermal Conductivity (Watts/cm K)	1.5	1.3	5	.11	24
Baliga FOM (W/cm^2)	$4.4 \cdot 10^7$	$3.5 \cdot 10^{10}$	$1.4 \cdot 10^{10}$	$1.4 \cdot 10^{11}$	$9.2 \cdot 10^{11}$

Table 1-1: Material parameters such as the relative permittivity, bandgap, critical electric field, electron mobility, saturation velocity and thermal conductivity [2, 3] of semiconductors of interest in the power industry. The Baliga Figure of Merit for each semiconductor has been calculated using equation 1.2.

In addition to a higher breakdown voltage and a lower on resistance, GaN also forms a spontaneous 2-dimensional electron (2DEG) gas at heterojunctions such as the GaN/AlGaN junction. The 2DEG transport mechanism in GaN allows higher mobility of carriers in GaN than in SiC or Si. The 2DEG is on the surface and so lends itself to a lateral device structure - as a result, all of the terminals are located on top of the device. SiC has a better thermal conductivity, making it a suitable candidate where the operation of the devices reach high temperatures. It lacks the ability to spontaneously form 2DEG junctions, however, and most implementations are vertical devices.

SiC substrates are more readily available at the time of this writing, and the quality is more uniform as compared to GaN free-standing substrates. GaN has been traditionally grown on sapphire, and occasionally on SiC or SiC. Thus, there is a higher dislocation density in GaN-on-heterogeneous substrate as compared to SiC-on-SiC. SiC has a slight advantage over GaN for very high voltage applications (i.e. above 600 V) due to lower defect densities (and subsequently lower costs) and a higher thermal conductivity. GaN is very suitable for medium power applications, and with progress in GaN-on-GaN epitaxy, the problem of defect densities

is expected to alleviate. GaN-on-Si is low in cost and can be extremely useful for low power applications (up to 200 V).

1.1 GaN Power Devices

GaN power device is a growing market and has the capability to be the displacement technology for Si in power conversion, RF, and analog applications. Emerging applications such as electric vehicle chargers find optimal results in GaN. It is the semiconductor of choice for power converters throughout vehicle electronics apart from the final drive inverter and there is now a very strong push to create production devices capable of switching as much as 100 A at 900 V [5]. The advent of mass adoption of electric vehicles may in turn push other major markets that depend on highly efficient high-density power converters. Currently, both lateral and vertical structures are being considered for GaN power devices.

1.1.1 Power HEMTs

Traditionally, High Electron Mobility Transistors (HEMTs) are the most common devices in GaN due to the spontaneous formation of a 2DEG in the GaN/AlGaN/InGaN system (figure 1.4).

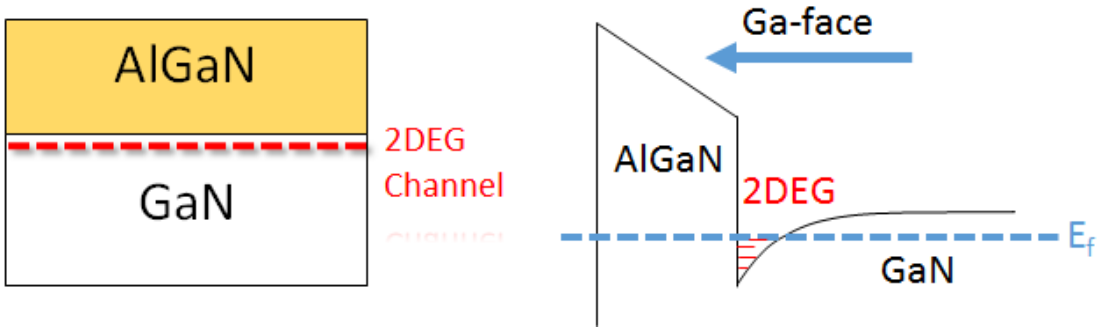

Figure 1.4: Schematic and band diagram of a Ga-polar AlGaN/GaN junction and the formation of 2-dimensional electron gas at its interface.

While most research in III-nitride optoelectronic and electronic devices had focused on materials and heterostructures grown in the Ga-polar direction [6], N-polar HEMTs, first demonstrated only a decade ago [7], offer several key advantages, especially for high power applications. In N-polar GaN HEMTs, the 2DEG is induced by a back barrier, rather than the top AlGaN layer. This natural back barrier enhances carrier confinement, and presents a barrier to electron injection into the buffer layer. The reduction in carriers injected into the buffer region improves the dynamic performance of the device, making the switching process more efficient. In addition to this, a well-insulated buffer layer from the channel increases the reliability of the transistor. Another advantage of the N-polar orientation for high voltage devices is the AlGaN cap, which maintains a high barrier to vertical electron transport. This, enhanced by the reverse polarity of N-Polar orientation, reduces the gate leakage, and thereby increases the breakdown voltage of the device.

Recently, N-Polar GaN Metal Insulator Semiconductor (MIS) HEMTs with multiple field plates have been reported [8] with breakdown V_{BR} ~ 2000 V and R_{ON} as low as 4mΩ.cm^2 (structure shown in figure 1.5). One drawback of the otherwise promising GaN MISHEMTs is that they are generally normally on, with a large negative threshold voltage V_{th}. This is due to

the presence of high-density positive polarization charges in the barrier layer (i.e. AlGaN back barrier). In D-mode (normally on) MISHEMTs, the gate rarely experiences forward bias during circuit operation, and subsequently experiences less adverse effects from the gate dielectric, such as Vth hysteresis.

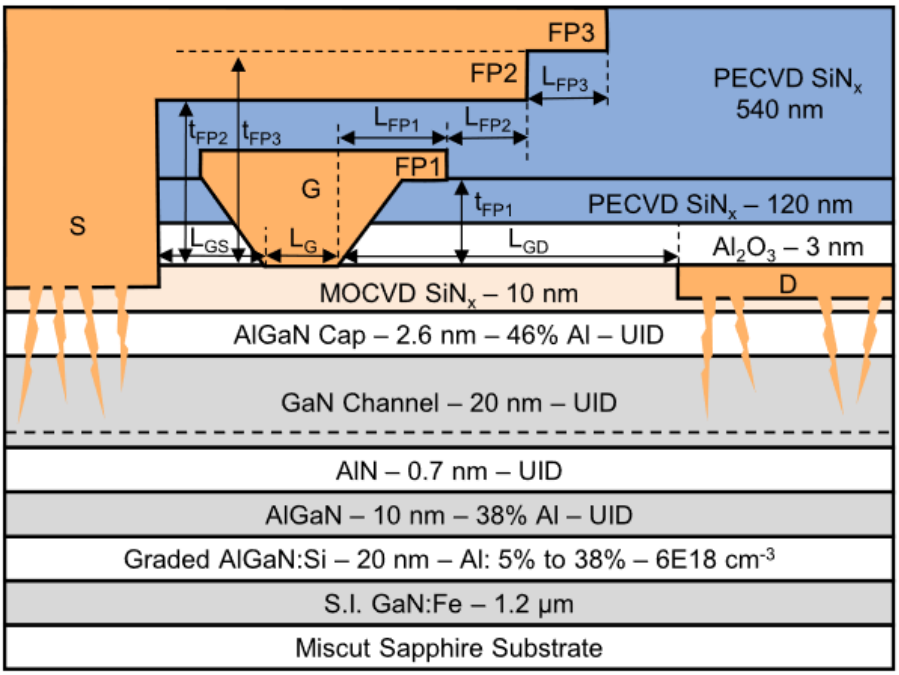

Figure 1.5: Structure of a multiple field-plated N-polar power HEMT. [8]

Trap states at the dielectric/AlGaN (or GaN) interface and inside the dielectric are the biggest challenge in GaN MISHEMTs [9] becoming more commercialized. Normally off or E-mode MISHEMTs with a positive V_{th} are highly desirable from the circuit application point of view for their simpler gate control and reliable operation. To fully turn on the channel current, however, large positive forward gate needs to be applied. This is when the gate dielectric is under the most demanding operational conditions such as high electric field, charge injection to the dielectric and carriers leaking through the dielectric. V_{th} instability, both static and

dynamic, at different temperatures and bias stress conditions, and its impact on dynamic R_{ON} needs to be systematically studied and clearly understood.

1.1.1 Vertical Devices

For applications where high currents and material-limited breakdown voltages are required, as well as applications where economics is important (i.e. a current density is required to lower costs), vertical device structures offer inherent advantages. Instead of having a long gate to drain length (L_{GD}) to hold the electric field (figure 1.6(a)) as in the case of lateral power transistors, a thick lightly n-type doped region or "drift region" can hold the electric field vertically (figure 1.6(b)) and prevent the device from getting large. Thus, vertical GaN power devices can deliver a high V_{BR} and a high I_{ON} without compromising on chip size. Other major advantages are superior reliability gained by moving the peak electric field away from the surface into bulk devices, and the easier thermal management than lateral devices.

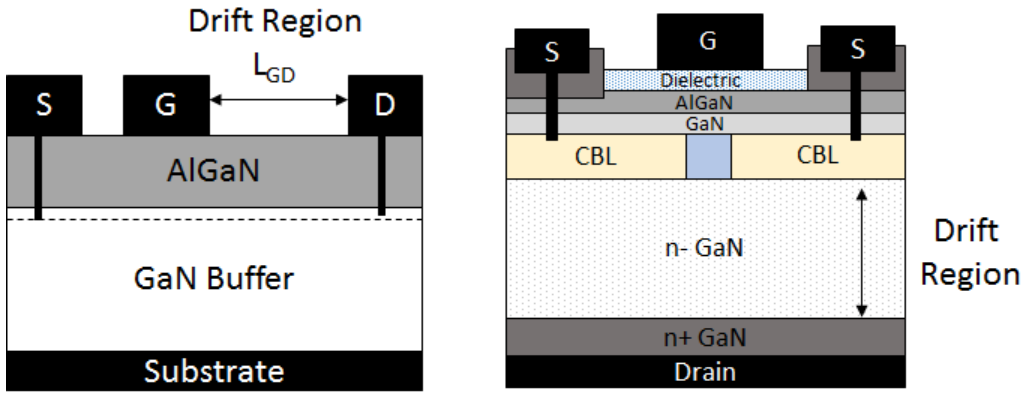

Figure 1.6: Structures of (a) lateral vs. (b) vertical power transistors. The drift region can be made thick in a vertical power transistor, controlling the area of the device.

A few examples of vertical GaN devices include the P-N diode (figure 1.7 (a)), the Current Aperture Vertical Electron Transistor (CAVET) (figure 1.7 (b)), the trench MOSFET (figure 1.7 (c)), the vertical channel JFET (figure 1.7 (e)), the vertical fin MOSFET (VFinMOSFET or MOSVFET) (figure 1.7 (f)), and the Oxide GaN-interlayer FET (figure 1.7 (d)). The CAVET combines the high conductivity of a two-dimensional electron gas (2DEG) channel (electron mobility up to 2000 cm^2/Vs and charge density ~ 10^{13} cm^{-2}) at the AlGaN/GaN heterojunction and an improved field distribution of a vertical structure. This type of structure is normally-on, but a trench semi-polar gate could allow for normally-off operation. All standard techniques that are currently used for rendering a lateral III-nitride HEMT normally off can be applied to a CAVET, but few reports are available.

Vertical GaN trench MOSFETs have no 2DEG channels, do not need the regrowth of AlGaN/GaN structures, and are intrinsically normally-off. JFET also offers a feasible solution for a normally-off device and has been studied considerably for both Si and SiC based power devices. Since the gate drive voltage in any JFET is limited to a maximum voltage equivalent to its bandgap, WBG materials, like SiC and GaN, have advantages over Si. SiC JFETs have demonstrated excellent performance in comparison to D-mode MOSFET. The first report on GaN vertical JFETs was published in 2015. To improve voltage tolerance in vertical JFET devices, an MOS modification has been proposed (VFinMOSFET or MOSVFET) and shown promising results. The Oxide-GaN interlayer FET (OGFET) is a modification of the Trench MOSFET, where a thin unintentionally doped (u.i.d) layer of GaN is grown beneath the oxide to provide better electron mobility in the channel.

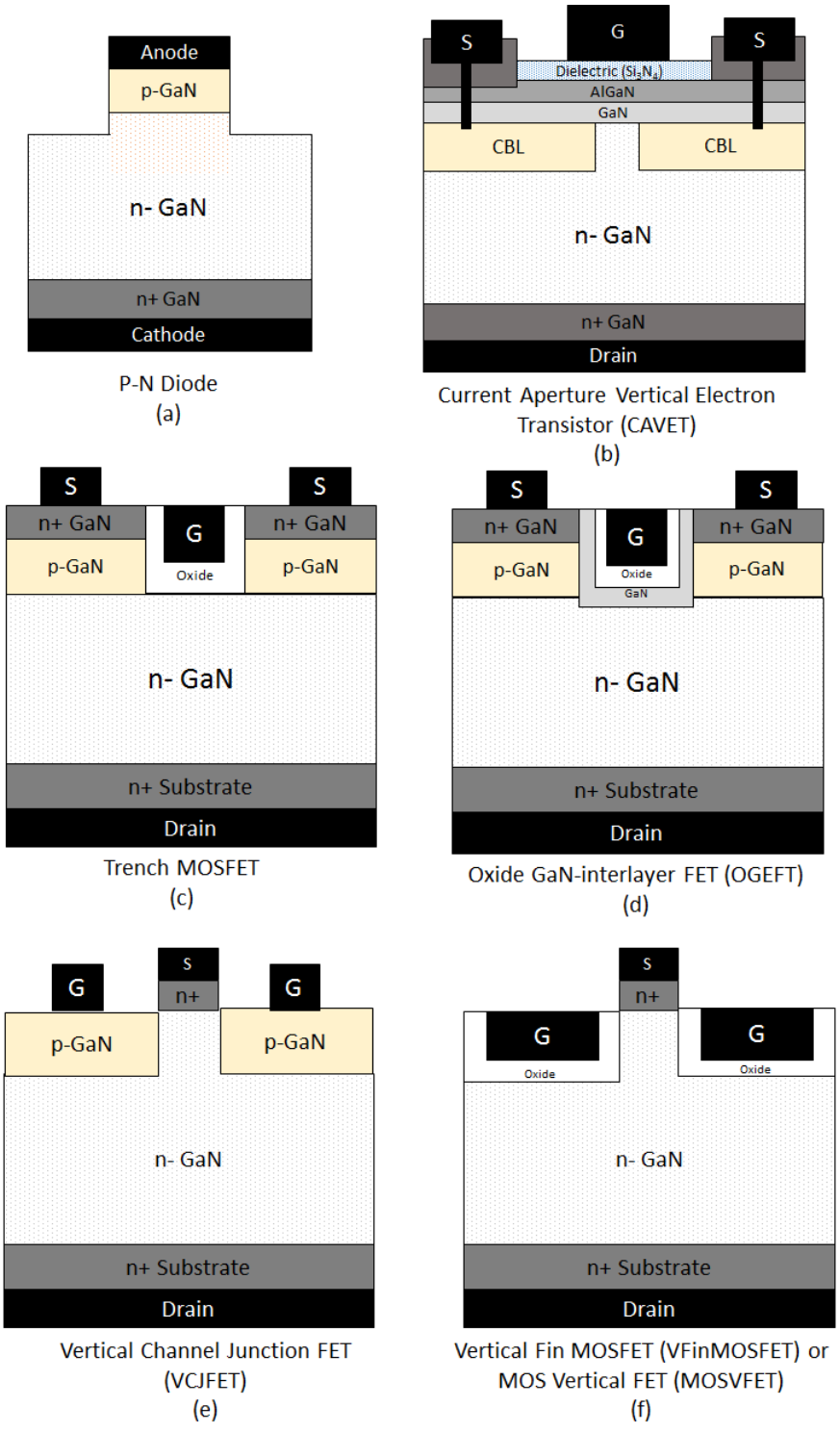

Figure 1.7: Different architectures of vertical GaN devices.

A trench CAVET (see figure 1.8) has also been demonstrated, that offers to circumvent MBE regrowth steps which are needed to suppress Magnesium diffusion into the channel region, replacing that with low-temperature MOCVD regrowth. The current blocking layer is also MOCVD growth p-GaN:Mg instead of implanted Mg. Thus, the entire device can be grown in the MOCVD while still maintaining a low channel resistance. Another added advantage is the increase in gate length. Table 1-2 compares the different types of vertical GaN transistors mentioned above.

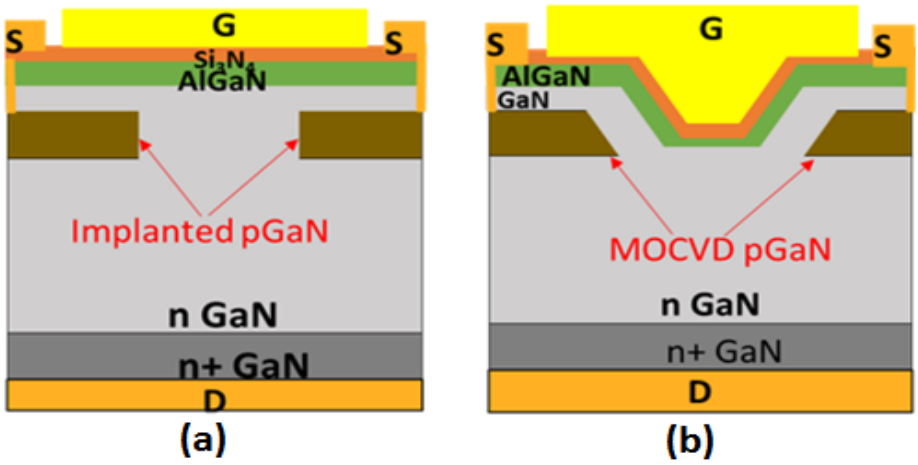

Figure 1.8: Schematic of (a) a conventional GaN CAVET with implanted p-GaN as the CBL and (b) the trench CAVET with MOCVD p-GaN as the CBL.

Structure	Advantage	Disadvantage
Current Aperture Vertical Electron Transistor (CAVET)	1. High channel conductivity due to 2DEG	1. Normally ON 2. Channel regrowth in MBE 3. Implanted Mg
Trench CAVET	1. High channel conductivity due to 2DEG 2. High gate length density 3. Better dielectric reliability as it can be grown in-situ via MOCVD	1. Normally ON 2. Channel can be regrown by MOCVD

Trench MOSFET	1. Normally OFF with threshold voltage > 3 V	1. High VGS required for device operation 2. Low channel mobility 3. Oxide reliability might not be good
Oxide GaN-interlayer FET (OGFET)	1. Normally OFF with threshold voltage > 3 V 2. Higher channel mobility and higher I_{ON} 3. Better dielectric reliability as it can be grown in-situ via MOCVD	1. High VGS required for device operation 2. Regrowth of GaN interlayer and oxide required
Vertical Channel JFET (VCJFET)	1. Normally OFF 2. No gate dielectric	1. Low gate bias tolerance (< 4 V) leading to low current density
Vertical Fin MOSFET (VFinMOSFET)	1. Normally OFF 2. No p-GaN regrowth 2. Higher gate biases can be tolerated due to the dielectric leading to higher current density	1. More complicated fabrication process

Table 1-2: A comparison of different vertical GaN structures. [11]

1.2 Other Materials for Power Devices

1.2.1 In the Market: Si and SiC

Silicon is by far the most widely used semiconductor material for power electronics with devices such as insulated gate bipolar transistors (IGBTs) [13] (see figure 1.9 (a)) and super junction MOSFETs [14] (figure 1.9 (b)). In a power MOSFET, a channel at the surface is inverted by the gate to create a channel just like in a typical MOSFET. Once electrons enter the drift region, the electric field from the applied V_{DS} causes them to drift towards the drain. To hold

a greater voltage, the drift region thickness can be increased. The tradeoff is an increased R_{on}. Thus, there is no merit in increasing the thickness of the drift region beyond the point where it stops benefitting the breakdown voltage. This drift region thickness limit can be calculated by expression 1.3:

$$w_d = \frac{E_{crit}\,\varepsilon_s}{q.N} \qquad 1.3$$

Super junction transistors are a modification of the power MOSFET, improving on the breakdown by juxtaposing p+ columns. This causes the field to be constant along this super junction, and the voltage to vary linearly. They can exceed the limit to breakdown described by expression 1.3. Another device design that can give higher breakdown voltages is the IGBT. The penalty is an increased threshold voltage and R_{ON}.

The primary markets hitherto have been very high power devices for infrastructure applications (~ 6600 V), medium power devices for home applications (100 – 240 V), and low power devices for personal applications (~ 12 V) [4]. Figure 1.10 shows the application arenas of different voltage and current ratings. It also shows the frequency of operation and power ratings of various types of Si power devices such as thyristors, IGBTs and MOSFETs. Despite great improvements, Si-based power devices are approaching their material limits. The maximum blocking voltage of the IGBT is lower than 6.5 kV, and the practical operating temperature is lower than 175 °C [16]. This has prompted a number of efforts to find alternatives to Si-based power devices for better performance.

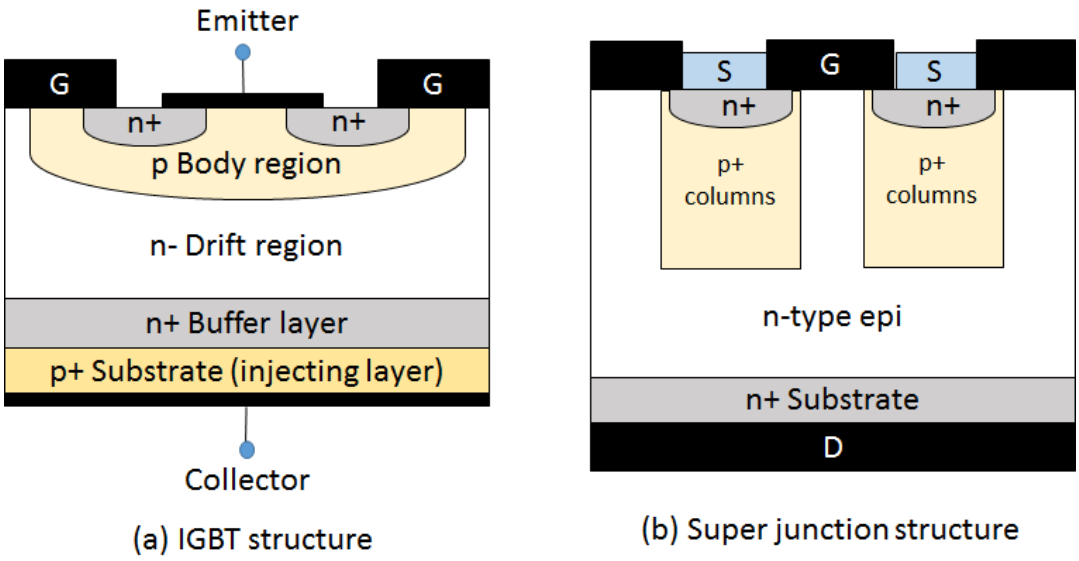

Figure 1.9: Cross-section of (a) a typical Si IGBT and (b) Super junction MOSFET.

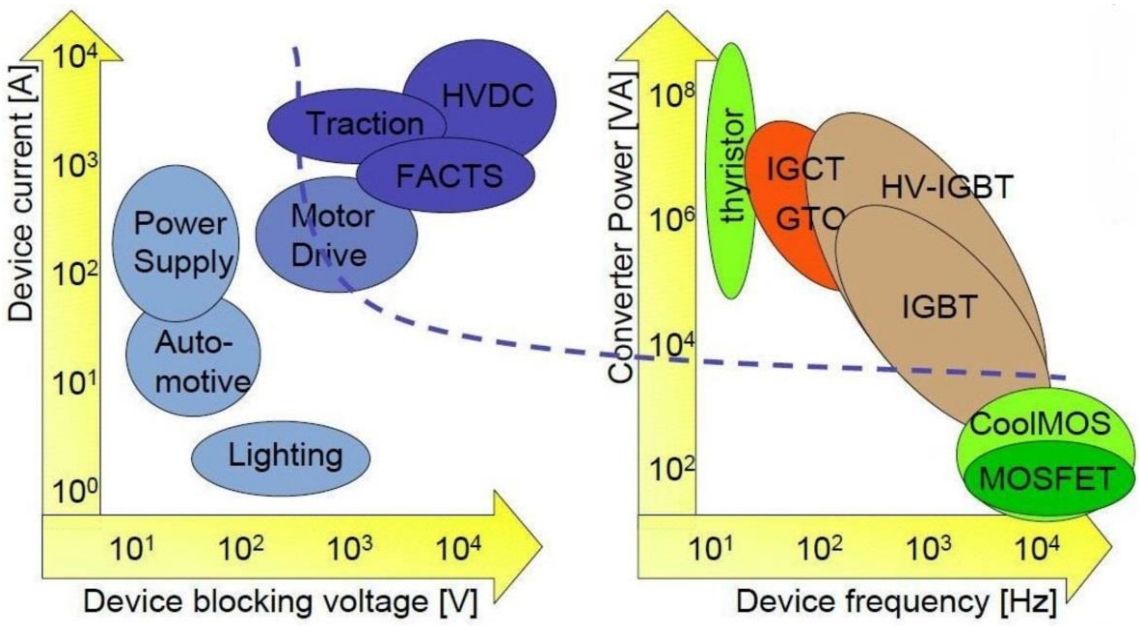

Figure: 1.10: Application fields of Silicon power devices. [10]

SiC is has gained prominence in the last two decades as an alternative to Si [12, 15]. It is the closest competitor of GaN in the current market. Its merits (see table 1-1) include a wider bandgap, higher thermal conductivity, and larger critical electric field. These allow SiC devices to operate at higher temperatures (well over 400 ^{o}C compared to 150 ^{o}C for Si), higher current density (2 - 3 times that of Si devices), and higher blocking voltages than Si power devices. Depending on the form of the crystal structure, the energy gap of SiC varies from 2.2 to 3.3 eV. 4H and 6H configurations are of interest technologically since large wafers can be made in this material, and hence used for device production. Even though several SiC power devices have been demonstrated, this technology is still at an early stage. Schottky diodes, JFETs, MOSFETs and BJTs are among the only SiC devices commercially available currently. Figure 1.11 gives a timeline of the SiC market development. Among the switches, JFET was the first SiC transistor to be commercialized. One major advantage of the JFET is its easy implementation and no oxide reliability issues. The drawback is that it is normally on, with a pinch off voltage of about -15 V. Normally off SiC JFETs with a turn-on of ~ 2 - 3 V have been made possible by adjusting the thickness and doping of the vertical channel, but the changes lead to a very high specific on-resistance ($R_{ON,SP}$). SiC MOSFETs were commercialized later than JFETs due to oxide reliability issues. The oxide degrades at temperatures even lower than the junction temperature. However, MOSFETs are still attractive due to being normally off. SiC BJTs have the lowest $R_{ON,SP}$ in theory and can operate at higher temperatures than SiC MOSFETs as there is no oxide layer. The drawback is that since it is a current controlled device, a continuous drive current is required to maintain the on status.

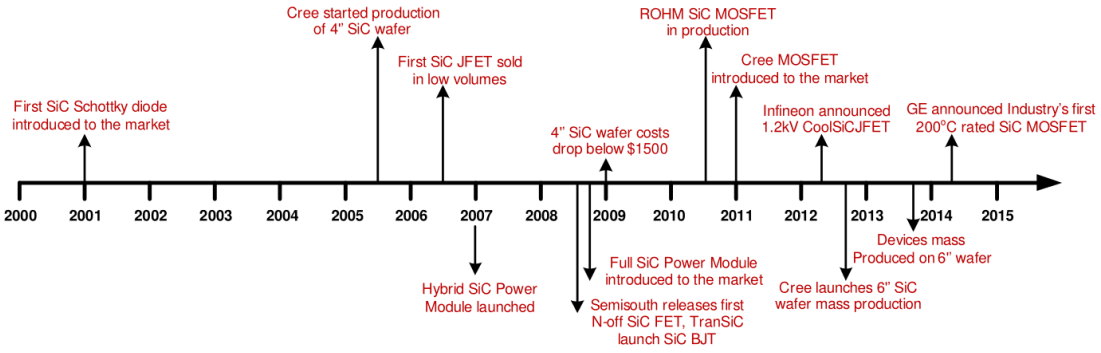

Figure 1.11: SiC device development milestones. [17]

1.2.2 Into the Future: Ga_2O_3 and Diamond

In recent times, gallium oxide (Ga_2O_3) has emerged as another promising candidate after GaN and SiC for power device performance.[18-20] Apart from its material property merits, it is also attractive from an industrial viewpoint since large-size, high-quality wafers can be manufactured from a single-crystal bulk synthesized by melt–growth methods. The β phase is most attractive as it is the most stable structure, while the other phases (α, γ, δ and ϵ) are metastable. Also, β-Ga_2O_3 is the only crystal structure that can be grown from the melt. The two primary drawbacks of Ga_2O_3 are a lack of p-type dopant and poor heat dissipation capacity. While n-type doping is easy with Sn and Si, there has been no report of successful p-type doping with effective hole conduction in Ga_2O_3. Also, the electron mobility is relatively low in Ga_2O_3. Growth of high quality thin films has been demonstrated by a number of different techniques, such as Molecular beam epitaxy (MBE), halide vapor phase epitaxy (HVPE), MOCVD and other CVD techniques. MBE is the most popular approach as CVD often leads to stacking faults, the reason of which is yet to be formalized. Devices such as MESFETs, MOSFETs and Schottky Barrier Diodes have been demonstrated on Ga_2O_3.

Diamond has a bandgap of 5.5 eV, higher than all other semiconductors discussed above. High electric breakdown, high mobility, and outstanding thermal conductivity make diamond one of the most suitable semiconductors for power devices. [21, 22] There are, however, many practical challenges to making a transistor work on diamond layers. Boron (acceptor) and phosphorus (donor) dopant atoms have a low ionization rates in diamond. This results in poor conductivity of the p- and n-layers, and a high series resistance. New device concepts have been researched and proposed to overcome these issues. Research on Field Effect Transistor (FET) solutions based on 2D hole gas has been done, such as: i) FET based on hydrogen terminated diamond surface [23-25], ii) FET based on AlN/diamond hetero-structure [26], iii) FET based on boron δ-doping concept (δ-FET) [27-29]. Boron δ-doped FETs consist of a highly doped thin layer of diamond sandwiched between two u.i.d layers. Quantum confinement causes delocalization of carriers near the δ-doped region and into the u.i.d region (due to wave function extensions). A gate bias on the surface parallel to the 2D hole gas allows to modulate the carrier density, thereby switching the FET to "on" or "off" states. The regular accumulation region ($V_G < 0$), weak inversion ($0 < V_G < V_{th}$), and strong inversion region ($V_G > V_{th}$) seen in enhancement mode MOSFETs has never been observed in diamond FETs due to poor interface quality between the dielectric oxide and the epilayer. Extensive research is being carried out to improve interfacial quality to improve diamond FET operation & characteristics.

1.3 Growth of III-Nitrides

Organometallic vapor-phase epitaxy (OMVPE) has been the technique of choice for III-nitride semiconductor growth or deposition of thin films for both academic, and industrial applications. In OMVPE, organometallic precursors and associated carrier gases are used for successful transport of the vapors of liquid and solid sources in the reaction chamber. Hydrides containing nitrogen are used for nitrides, and they react on the surface of the heated substrate where deposition of thin films occur. The most commonly used group III precursors include trimethylaluminium, trimethylgallium, triethylgallium, trimethylindium etc. The stability of these molecules is highest for Al, and lowest for In containing organometallics. The normal growth temperature (substrate temperature) for III-nitride films range from 1100 to 600 °C. The common donor and acceptor dopant sources are the Si-containing hydride gases like silane, and the organometallic cyclopentadienylmagnesium, respectively.

Substrates are an important consideration in the growth of III-nitride films. Electronic and optoelectronic devices made from III-nitride layers have multiple layers of nitrides of different Ga, In, Al compositions, and as such have different amount of strain. Choice of substrate plays a critical role since GaN is expensive, and other substrates of choice are cheaper, but have larger lattice mismatch like SiC, sapphire and Si. As such nitride layers grown on top of foreign substrates are extremely sensitive to strain, one-dimensional (dislocations) and two-dimensional (stacking faults, anti-phase boundaries, etc.) defects, and unintentionally induced impurities.

Extensive research on growth mechanisms of [0001]-oriented GaN, InGaN, AlGaN layers have been performed as they have relatively large growth window (pressure, temperature, precursor flow) compared to other polar & semi-polar orientations of GaN (figure 1.12). However, [0001]-oriented GaN has large piezoelectric strain and associated internal

electric field which significantly degrades radiative efficiency, and thereby performance characteristics of optoelectronic devices. Because of better growth window, [0001]-GaN is still the preferred orientation of growth, and novel device structures and bandgap engineering is carried out to handle the piezoelectric strain.

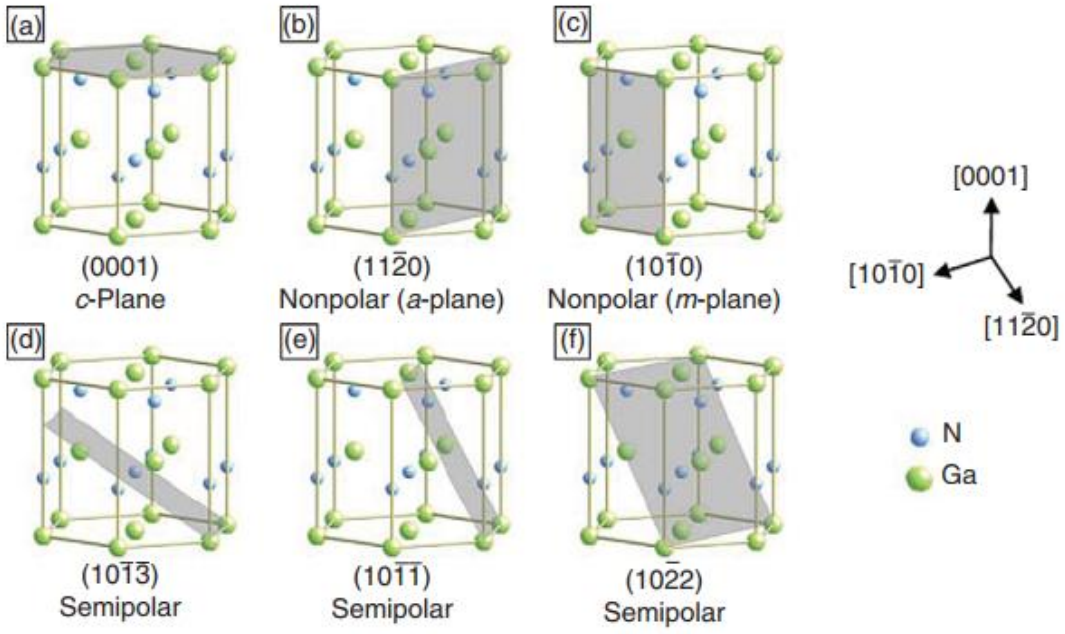

Figure 1.12. Schematic illustrations of (a) the polar c-plane (0001), (b) the nonpolar a-plane (1120), (c) the nonpolar m-plane (1010), and (d)–(f) the semipolar planes (1013) (1011), and (1122), respectively.[30]

Sapphire is a readily available foreign substrate which is used extensively for developing growth conditions of III-nitrides, and also making device prototypes. However, the lattice and thermal coefficient mismatch between GaN and sapphire along [0001] direction is 13.9% and 25.3%, respectively which is huge for considerations of epitaxial growth. Hence, GaN growth on sapphire is very challenging. GaN directly grown on sapphire have very large Full Width Half Maxima (FWHM) of X-Ray Diffraction (XRD) peaks (15-30 arcmin), high

residual electron concentrations (> 10^{18} cm^{-3}), and 3-D morphologies with RMS roughness > 10 nm.[31] Buffer layers have been used to prevent poor quality GaN growth on sapphire. Nitridation of sapphire substrates to grow a very thin layer of AlN that lowers the lattice mismatch with subsequently grown on GaN layers have been performed. However, there is an optimum thickness and growth condition of AlN nitridation layer for best quality subsequent GaN layers. The role and importance of buffer layers in the subsequent GaN epitaxial film growth quality have been extensively characterized and researched. [32, 33, 34] Initially, a high density of GaN nuclei is formed (figure 1.13(a)) that grows preferentially and laterally along the <112'0> family of directions (figure 1.13(b)). Small flat-topped, hexagonally shaped, three-dimensional islands form and rapidly coalesce (figure 1.13(c)) until the entire surface of the nucleation layer is covered (figure 1.13(d)). The control of island size (or island density) in the initial stage of growth of these films plays an important role in the reduction of the threading dislocation (TD) density as well as the improvement of surface microstructure. The island density of the high temperature (HT) GaN is strongly dependent on the V/III ratio, reactor pressure, and the chemistry of the carrier gas. Generally, the larger the nominal diameter of the HT-GaN islands, the lower the density of TDs in the thicker GaN layers. A very high V/III ratio (> 2000) is generally used to grow GaN films via OMVPE in H_2. Al*x*Ga1*x*N films can be grown over the whole range of compositions via OMVPE at low pressures (0 – 100 torr.) using ammonia, TMA, and either TEG [35] or TMG [36]. The optimum growth temperatures range from 1000 (GaN) to 1130 °C (for all solid solutions above x = 0.50) [35]. $Al_xGa_{1-x}N$ solutions with x < 0.5 grown via OMVPE must be deposited at a temperature of about 1060 °C, because the sticking coefficient of Ga is much lower than Al, and the incorporation efficiency of the former component at higher temperatures is progressively

reduced. High N/metal ratios within the temperature range of 750 – 800 °C are used to obtain the optimum microstructures and dislocations densities for $In_xGa_{1-x}N$ growth.

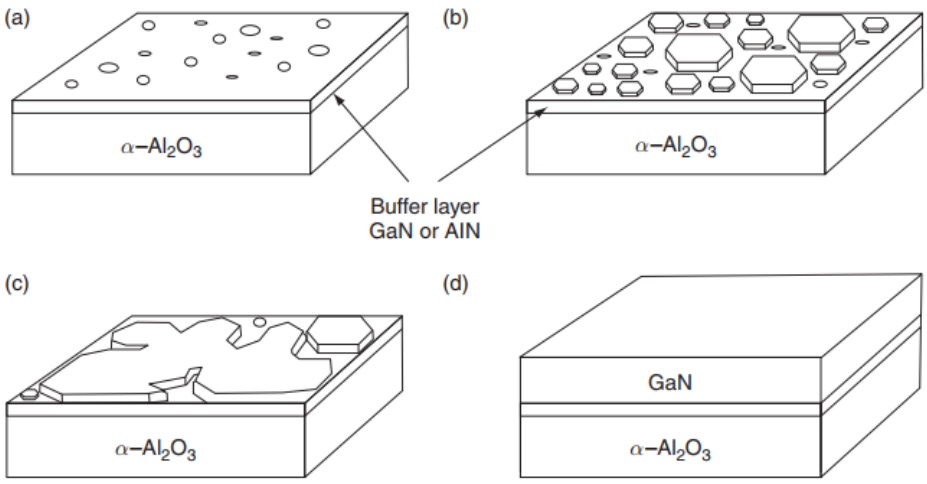

Figure 1.13. Mechanism of coalescence of hexagonal islands that results in 2-D growth of a GaN film deposited on a buffer layer previously grown on a (0001) sapphire substrate. [37]

1.4 Growth for Vertical Architectures

Vertical architectures are desirable for high V_{BR} and I_{ON} applications. However, these devices also place additional demands on material quality. While high dislocation densities are often tolerable in optoelectronic and lateral electronic nitride devices, these defects significantly compromise the performance of vertical devices. Homo-epitaxy is thus highly desirable for vertical power devices.

A common feature of most GaN vertical devices is the need for a low n-type doped drift region (see figure 1.14). This can be difficult to achieve due to the background Carbon

and Oxygen levels in the MOCVD reactor. Moreover, this doping level should be uniform and achieved consistently.

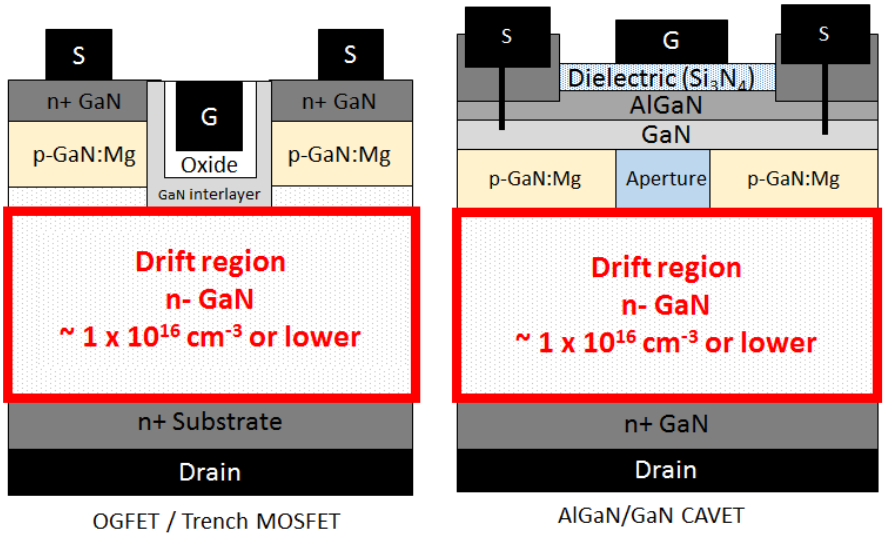

Figure 1.14: GaN vertical devices have a thick low-doped drift region to enable high breakdown voltages. This can be challenging to grow in the MOCVD.

Another issue is the diffusion of Magnesium into nearby, especially subsequent layers of GaN, as Mg is highly unstable at high growth temperatures. Mg is the only known p-type dopant of GaN and it is a challenge to regrow on p-GaN in all types of GaN devices. Even though techniques such as wet etching, regrowth via MBE, or AlN interlayers can be used, it is preferable if a solution can be developed in-situ within the MOCVD reactor to save additional steps. Examples of p-GaN in our vertical devices is shown in figure 1.15.

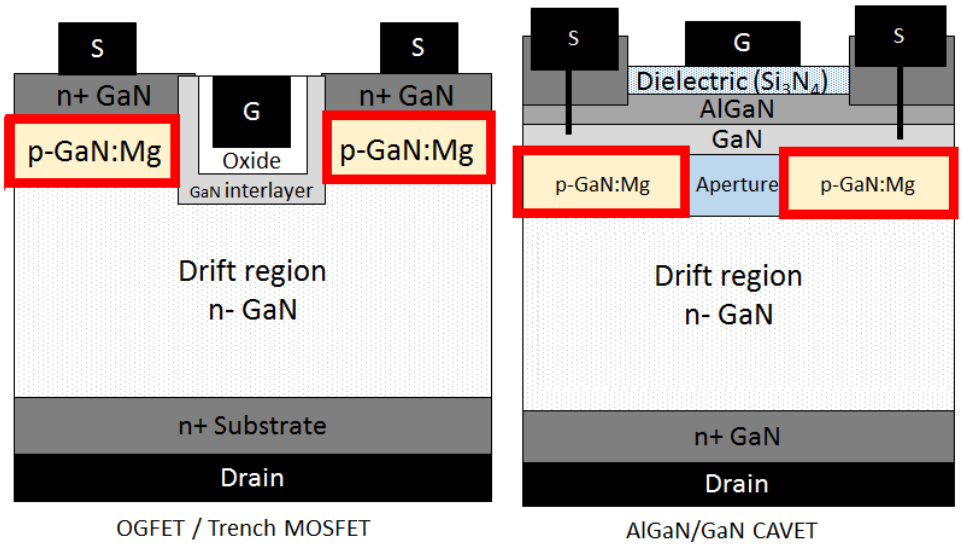

Figure 1.15: Magnesium doped p-GaN or implanted Magnesium in GaN tends to be highly unstable at high growth temperatures and diffuses into surrounding layers, leading to lowered device performance.

Regrowth on patterns is another challenge for our vertical devices. Regrowth for various trench dimensions has been optimized in this thesis. This includes both, conformal regrowth and filling of trenches (see figure 1.16).

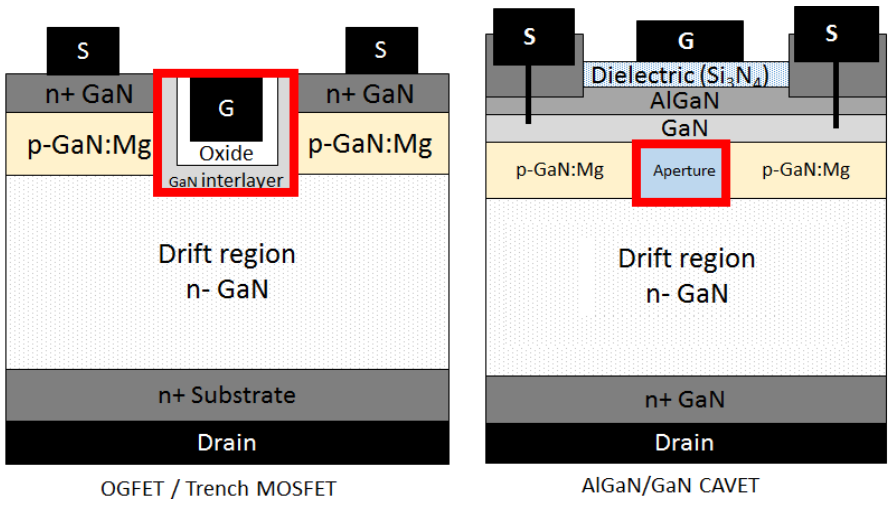

Figure 1.16: Devices often have different regrowth requirements in terms of the desired geometry, such as conformal regrowth or planarizing the surface.

1.5 Overview of Chapters

This dissertation aims to serve as a handbook to future researchers and students in the field of power GaN devices, especially vertical devices. It is heavily focused on the growth aspect of GaN power devices, using the Metal Organic Chemical Vapor Deposition (MOCVD) technique. The first challenge in vertical GaN devices is the growth of uniformly doped n-type drift regions. This is a common feature in all the vertical devices discussed above. The drift region has to be doped extremely low (1 x 16 cm^{-3}) for an optimum R_{ON} and V_{BR}. Chapter 2 discusses how the Carbon and Oxygen background dopant levels were suppressed and consistent low doping was achieved. P-N diode results, both on sapphire and bulk GaN substrates, have also been presented. Magnesium is the only feasible p-type dopant for GaN, but due to its small atomic size, it tends to be highly unstable at the high growth temperature of MOCVD GaN causing issues in device performance. Chapter 3 deals extensively with demonstrating a novel approach to Magnesium suppression in GaN using MOCVD. Chapter 4 delves into maskless regrowth conditions for GaN to get the desired geometry in trenches. AlGaN regrowth has been proposed to lower gate leakage in deep recessed gate HEMTs. Chapter 5 presents the preliminary results for this proposal. Two MOCVD reactors at UCSB were used for growth. MOCVD 4, which is the single-holder Thomas Swan tool, has been used for most of the growths in this thesis. The other reactor, MOCVD 5 (Nippon Sanso), was used primarily for all the growths on bulk GaN.

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2 Buffer and Drift Layers in Vertical Devices

GaN based vertical devices offer strong electric fields in the bulk of the nitride crystal rather than along the surface, giving the device a capacity to hold very high electric fields. [1] A high V_{BR} enables high power operation while the low R_{ON} enables efficient power conversion. As discussed in chapter 1, examples of vertical GaN devices include the p-n diode [4], and various modifications of the CAVET [2] and the trench-gate MOSFET [3]. The AlGaN/GaN CAVET structure has been successfully demonstrated using an Mg implanted current blocking layer [5], but the drift layer is yet to be optimized for high breakdown voltages. Through simulations, it has been shown that for fast switching, a high V_{BR} and a low R_{ON} to be simultaneously achieved, the drift region must be n-type doped at a level of around 1 x 10^{16} cm^{-3} or lower [6]. This is a common and key feature of vertical power devices. The free electron concentration in u.i.d materials corresponds to the difference between residual donors and acceptors in the crystal. While u.i.d GaN has typical carrier concentration levels of 1 x 10^{16} cm^{-3} (primarily C and O), it is an unreliable and unreproducible method to achieve low concentrations. Thus, it is useful to be able to control n-type doping levels using a dopant (such as Si) to get unvarying results. Low doping levels using Si as the dopant is, however, difficult to control as any change in growth conditions has a significant impact on the unintentional

dopants at these low levels. Carbon is inherently supplied by the organic gallium precursor, trimethylgallium Ga-$(CH_3)_3$ and assumes a deep-acceptor state in GaN [7, 8]. Oxygen typically behaves like an n-type dopant [9, 10]. Growth conditions which suppress the incorporation of residual O and C impurities include a combination of high growth pressures, high growth temperatures, and high V/III ratios.

2.1 Buffer Layer

Due to the unavailability of high quality GaN substrates, GaN has been mostly grown on sapphire or SiC substrates until very recently. Even now, GaN substrates are very expensive, running into thousands of dollars for a 4" wafer. Before the discovery of buffer layers, the quality of GaN films was poor. The surface was rough, and had numerous cracks due to the large lattice and thermal mismatches between GaN and sapphire. In the late 1980s, Amano et al. [25] were able to improve the quality of epitaxial GaN by pre-depositing a thin AlN buffer layer before the growth of GaN. Further progress was made by Nakamura et al. [26] While GaN was grown at a typical temperature of ~ 1050 °C, the buffer layer was grown at a lower temperature between 450 °C and 600 °C, and the thickness was varied between 100 and 1200 Angstroms. Figure 2.1 shows the microscopic images of the surface for different buffer layer growth times. The smoothness improves tremendously with the buffer layer growth time (translating to higher thickness). Thus, all growths on sapphire include a buffer layer under the layers of interest.

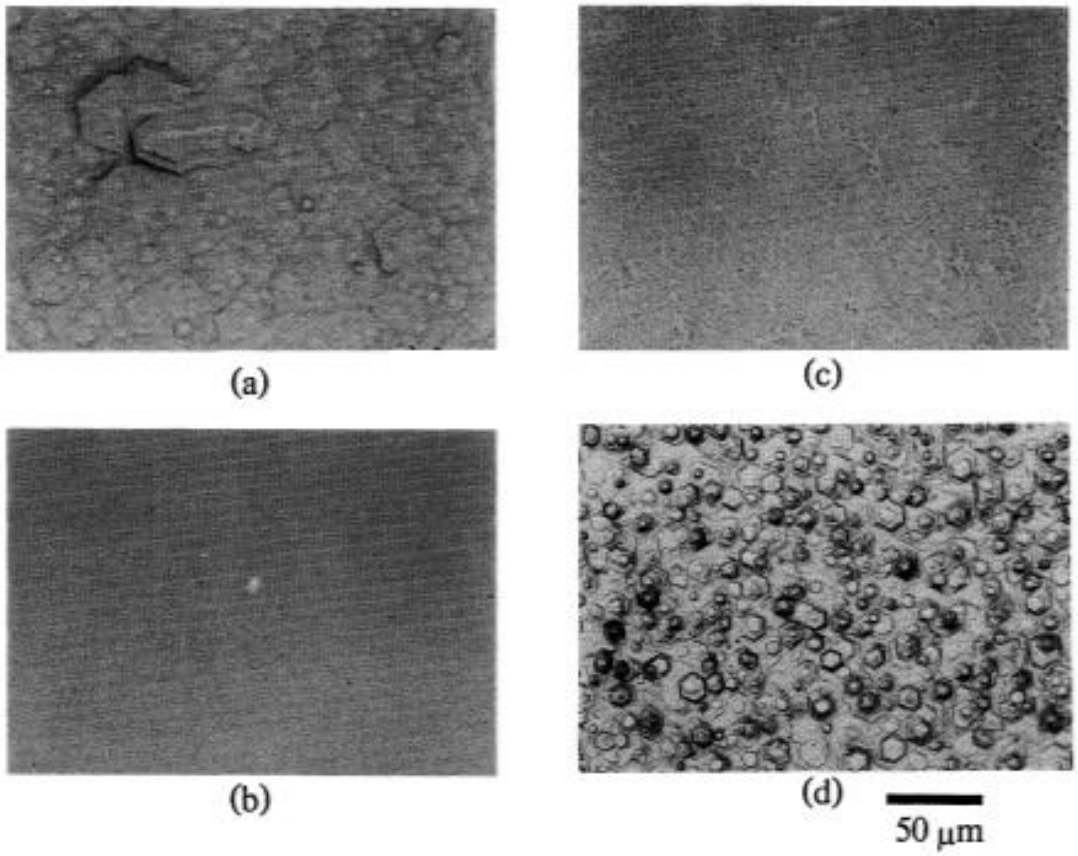


Figure 2.1: Images of the surface of GaN films grown by Nakamura et al. with buffer layer growth times of (a) 30 secs, (b) 70 secs, (c) 90 secs and (d) 0 secs. [26] The morphology improves with increased growth times.

2.2 Low Doped Drift Layers

2.2.1 Drift layers on sapphire substrates

All samples in this study were grown on c-plane sapphire substrates using TMGa, NH_3, ferrocene and disilane as precursors. The Si doping was evaluated using 'MESFET-like' test structures (as depicted in figure 2.2) which were evaluated by Van der Paw Hall measurements. The samples were composed of a 1 μm GaN:Fe layer followed by a 3 μm thick unintentionally

doped GaN layer and then the GaN:Si layer. 2.5 µm of this u.i.d layer was grown at a high growth rate (42 nm/min) and the rest was grown at 27 nm/min. This was to ensure that the Fe concentration was sufficiently low in the GaN:Si layer. The GaN:Si layer was also grown at 27 nm/min to reduce the C brought in by metalorganic sources (TMGa or TEGa). This layer was 2 µm thick for the higher doped samples (all the way down to 1 x 10^{16} cm^{-3}) and 3 µm for the lower doped samples (5 x 10^{15} cm^{-3} and 2 x 10^{15} cm^{-3}), to enable a decent sheet resistance value. The same structure without any DiSi flow in the top layer was measured to be semi-insulating, ensuring that any charge measured in the doped layers originated from the Si and not from unintentional impurities. A high temperature (1190 °C), a high pressure (600 torr.), and a high Ammonia flow (6 SLM) was used for all growths. The Si doped test structures were characterized by Hall measurements at room temperature. To check the film quality, an X-Ray ω-scan was performed using the X'pert Epitaxy software. The morphology was inspected by Atomic Force Microscopy using a Dimension 3100 Nanoman AFM from Veeco.

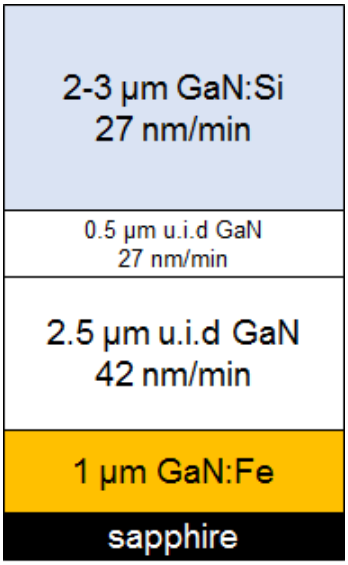


Figure 2.2: Test structure for Van der Pauw Hall measurements.

The p-n diode series was grown with carrier concentrations ranging from ~1 x 10^{16} cm^{-3} down to 2 x 10^{15} cm^{-3}. The growth conditions used for the GaN:Si layers were identical to those used for the Hall structures. A thickness variation series – 3 μm, 6 μm and 8 μm - was also grown. Thicker n- regions are expected to have significantly higher breakdown voltages. The epitaxial layer structure (see figure 2.3(a)) consisted of a 2 μm of highly doped (2-3 x 10^{18} cm^{-3}) n-type GaN for contacts followed by a thick drift region (3/6/8 μm thick) of low doped GaN and 400 nm of p-GaN (Mg: ~7 x 10^{19} cm^{-3}). Activation of GaN:Mg was performed in N_2/O_2 ambient environment at 700 °C. The device fabrication process (see figure 2.3(b)) started with the deposition of Ni/Au (200 nm) as ohmic contacts to the p-GaN layer (anode). In order to access the highly conductive n-type doped layer and achieve mesa isolation, a deep GaN etch was performed. Using the top contact (Ni) as hard mask, a high power $Cl_2/Ar/BCl_3$ gas combination etch was done in the inductive coupled plasma (ICP) system. The isolation etch on the sidewall was a low damage etch in order to avoid a large parasitic leakage current. A large area (2 mm x 2 mm) Al (25 nm)/Au (250 nm) contact was deposited on the exposed n-layer for the cathode. Large area contact was deposited to minimize the contact and the drift resistance due to contact being placed on the n^-- GaN layer.

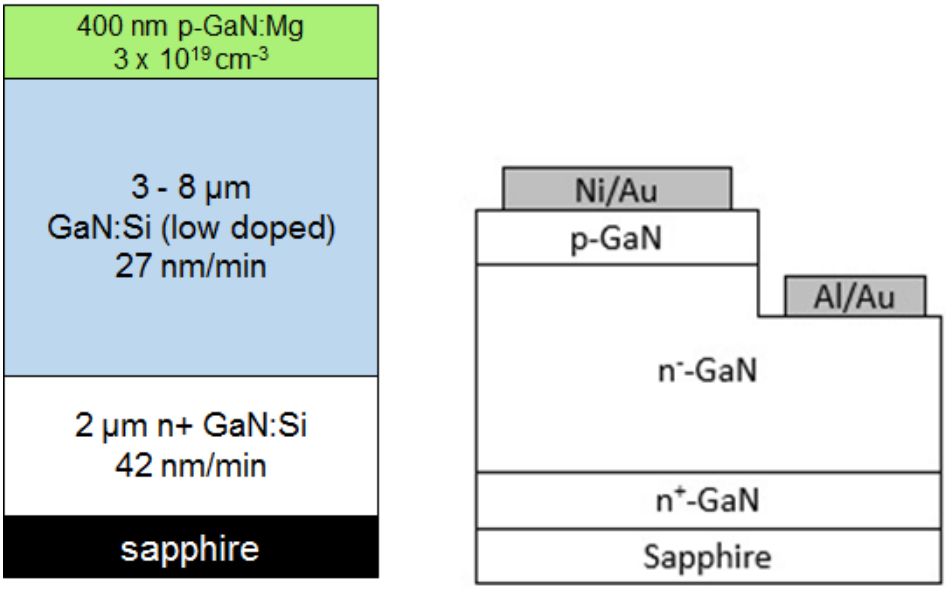


Figure 2.3: (a) The structure for diode measurements and (b) the processed p-n diode.

The disilane (Si dopant) flow was scaled for different doping levels starting from ~1.24 x 10^{18} cm^{-3} down to ~5 x 10^{15} cm^{-3} for the hall structures and from 1 x 10^{16} cm^{-3} to 2 x 10^{15} cm^{-3} for diodes. The trend was linear (see figure 2.4). The electron mobility seemed to follow a bell curve, peaking at 899 $cm^2V^{-1}s^{-1}$) for carrier concentrations of 1-2 x 10^{16} cm^{-3} and falling to <600 $cm^2/(Vs)$ for lower concentrations. All Hall measurements were done at room temperature. In the sample with the very high mobility of 899 $cm^2V^{-1}s^{-}1$, the FWHM for the (0 0 2) symmetric rocking curve (ω-scan) was 222.8 arcsec. That for the (2 0 1) X-ray diffraction peak was 502 arcsec. These indicate threading dislocation densities in the epitaxial layer- in the mid ~10^8 cm^{-3} level [11]. This dislocation density range was confirmed by AFM (see figure 2.5). The high electron mobility achieved in this study is attributed to optimum growth conditions. The decrease in electron mobility at a doping level below 1 x 10^{16} cm^{-3} could be due to the reduced screening of threading dislocations at these low carrier concentrations. Low

n-type doping (1 x 10^{16} cm^{-3}, 5 x 10^{15} cm^{-3} and 2 x 10^{15} cm^{-3}) was extracted from processed p-n diodes (see figure 2b).

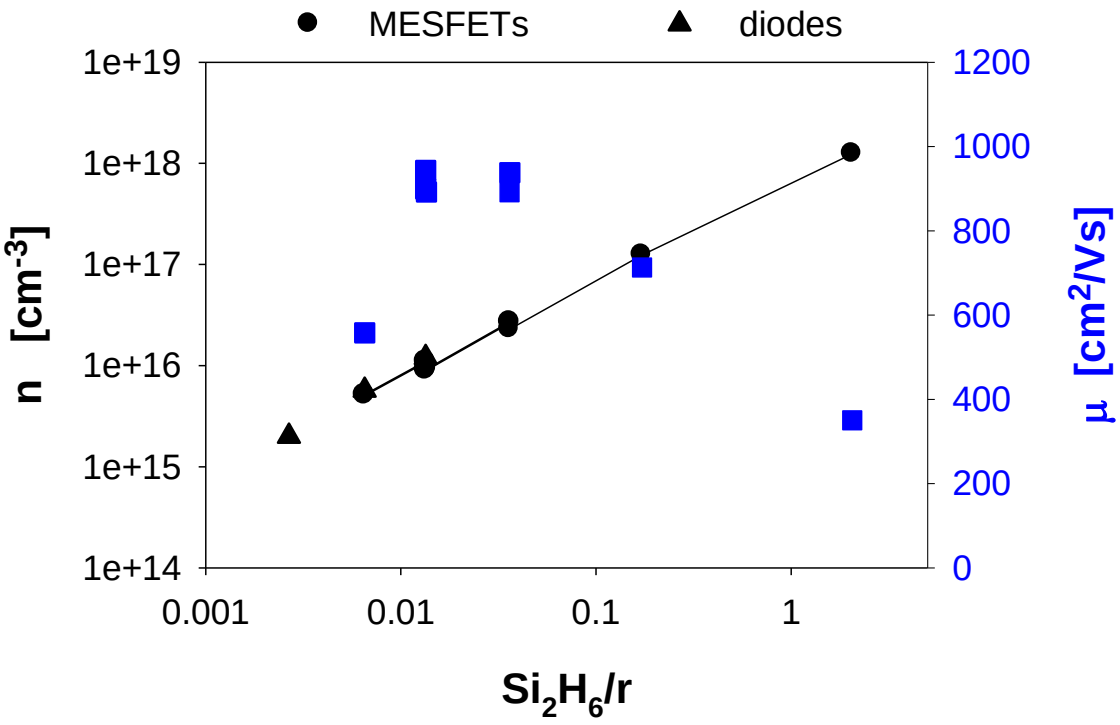


Figure 2.4: Hall and diode results from the low doping series.

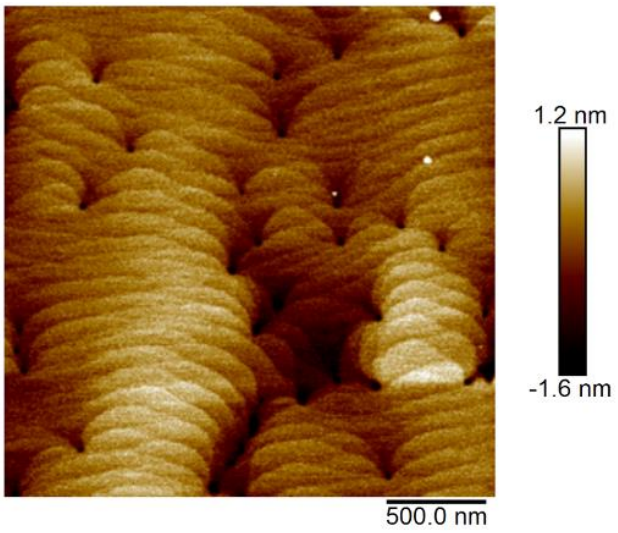


Figure 2.5: AFM scan of the high mobility test structure (1 x 10^{16} cm^{-3}).

Samples with doping levels varying from 1 x 10^{16} cm^{-3} to 2 x 10^{15} cm^{-3} and thicknesses varying from 3 μm to 8 μm were tested. The p-n diode forward and reverse I-V curves are shown in the figure 2.6 and figure 2.7 respectively for 6 μm thick, 1 x 10^{16} cm^{-3} doped sample. The on-resistance dependence on drift region carrier concentration and thickness is shown in figure 2.8. Since, the major target of the diode study was to obtain p-n junction breakdown, the forward characteristics weren't optimized. The large area n-type contact was placed at a distance of few centimeters from the anodes to avoid surface breakdown of the diodes which resulted in increased series resistance. Here, the on-resistance was calculated by excluding the series resistance. As expected, the on-resistance increased with drift region thickness for same carrier concentration. Also, for same drift region thickness, on-resistance increased with decreasing carrier concentration. Lowest on-resistance was observed with 1 x 10^{16} cm^{-3} doped sample due to higher mobility and higher charge. The breakdown voltage in this study is defined as the voltage at which reverse leakage current density crosses 0.1 A/cm^2 [12]. There was an expected increase in breakdown voltage with decreasing doping level in the samples - from 640 V for the 6 μm, 1 x 10^{16} cm^{-3} sample to 890 V for the 6 μm, 2 x 10^{15} cm^{-3} sample (see figure 2.9). The breakdown voltage almost doubled when the thickness of the drift layer was doubled from 3 μm to 6 μm for the tested doping levels. It was not possible to measure the 8 μm sample with 2 x 10^{15} cm^{-3} doping as our measurement limit was reached (> 1000 V). This is the highest breakdown voltage achieved in GaN on sapphire to the best of our knowledge [12, 13]. It is possible to get higher breakdown on bulk GaN as displayed by Nie et al. [14] who achieved 1.5 kV, but in addition to the use of low treading dislocation density bulk GaN substrates their drift region thickness was 15 μm as opposed to 8 μm (the thickest sample tested in this study).

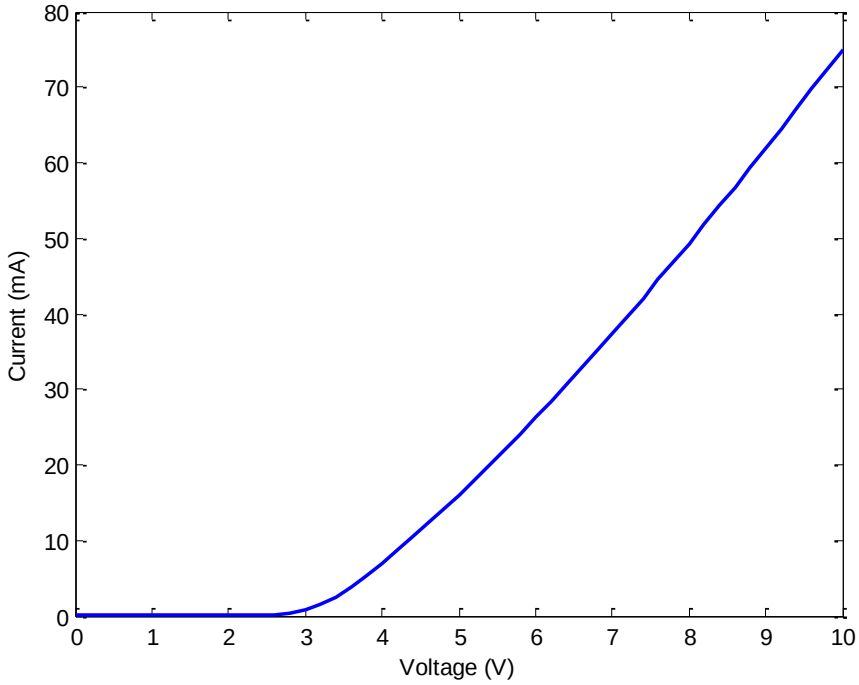


Figure 2.6: Forward I-V characteristics of p-n diode (100 μm diameter).

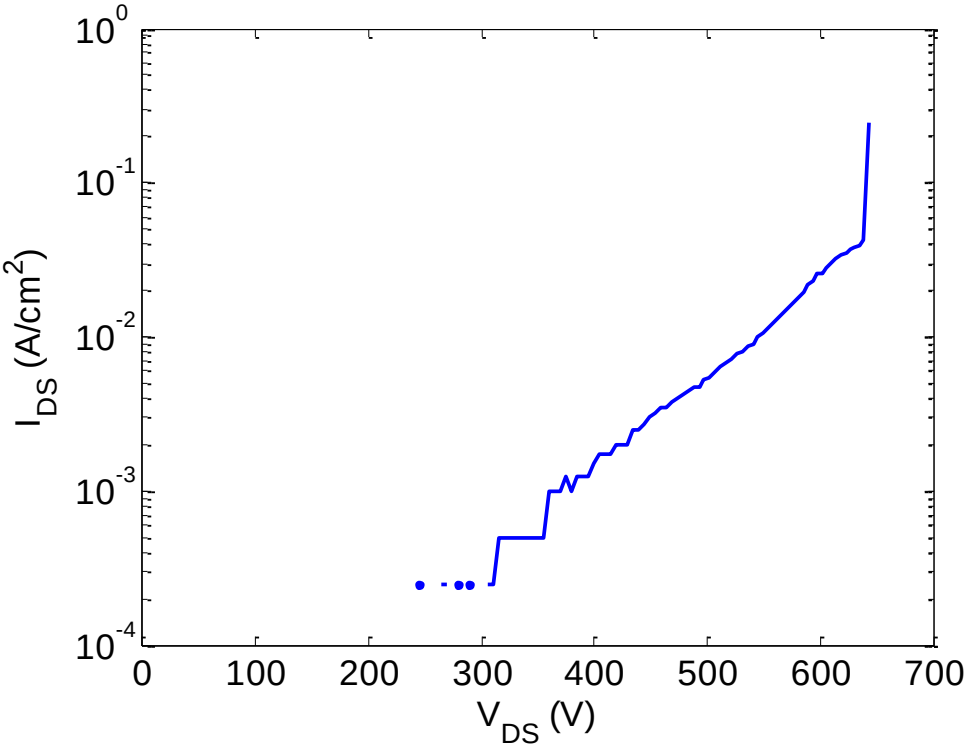


Figure 2.7: Reverse I-V characteristics of p-n diode (100 μm diameter).

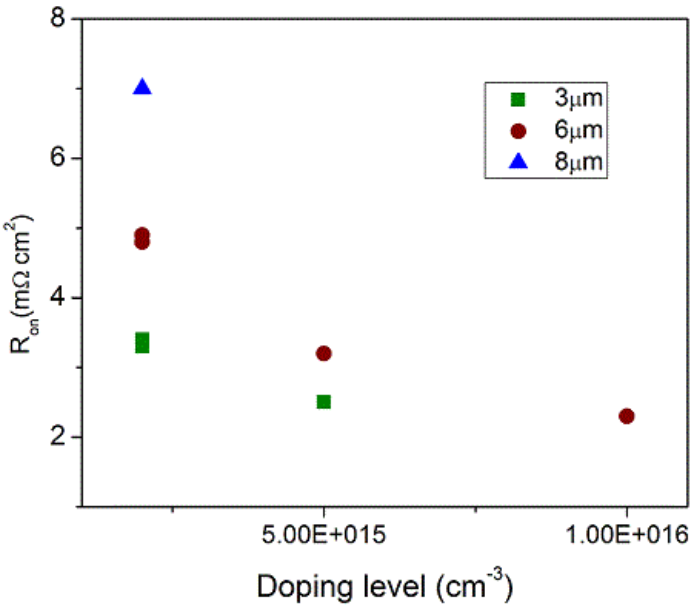


Figure 2.8: N-type carrier concentration and drift layer thickness Vs R_{ON} for p-n diodes on sapphire.

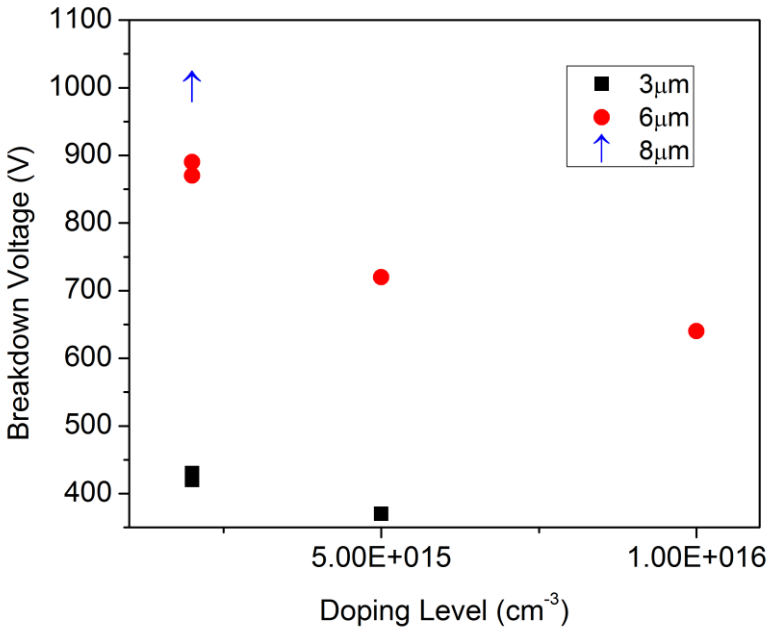


Figure 2.9: N-type carrier concentration and drift layer thickness vs. V_{BR} for p-n diodes on sapphire.

2.2.2 Issues with carbon incorporation

We experienced a carbon incorporation problem when using MOCVD 4 for growths on bulk GaN substrates, rendering the drift layers semi-insulating [27, 28]. The reason is yet unknown, but might be due to the bulk GaN substrates being n+ (in the 10^{18} cm^{-3} range), while the sapphire substrates used were always insulating. This issue was resolved by using MOCVD 5 for GaN-on-GaN growths. We used the unintentional C incorporation as an opportunity to study how it changed for different growth rates and temperatures (SIMS results in figure 2.10). As expected, C incorporation increases greatly at higher growth rates as there is less time for C to desorb from the surface. C incorporation reduces slightly at higher growth temperatures. Figure shows the SIMS result for a co-loaded sapphire piece in the same run. The C levels are below detection limits for the sapphire piece (figure 2.11), so the variations with temperature and growth rates cannot be seem.

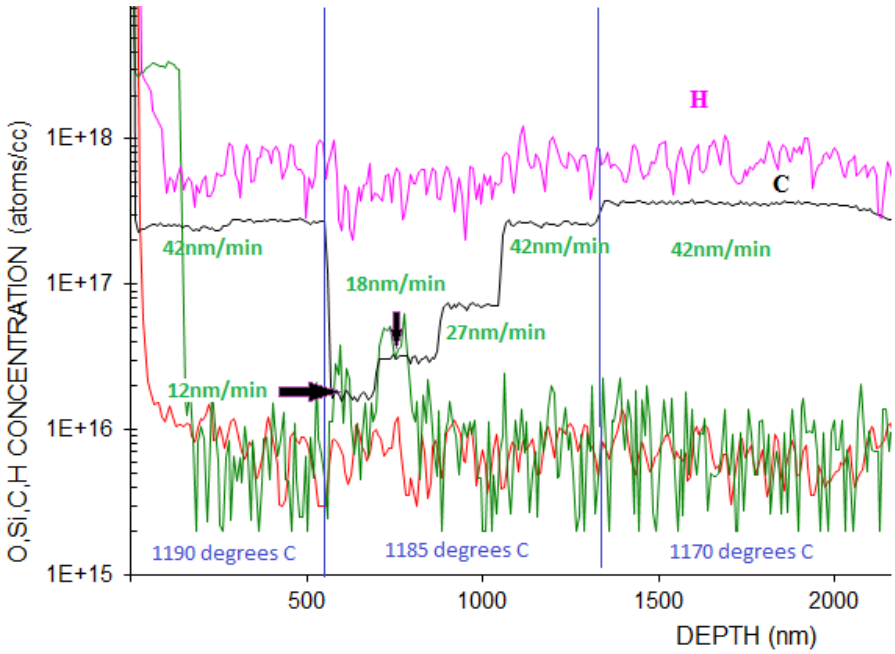


Figure 2.10: SIMS results for carbon incorporation in MOCVD GaN (Thomas Swan) as a function of growth rate and temperature. Carbon incorporation increases at lower temperatures and higher growth rates.

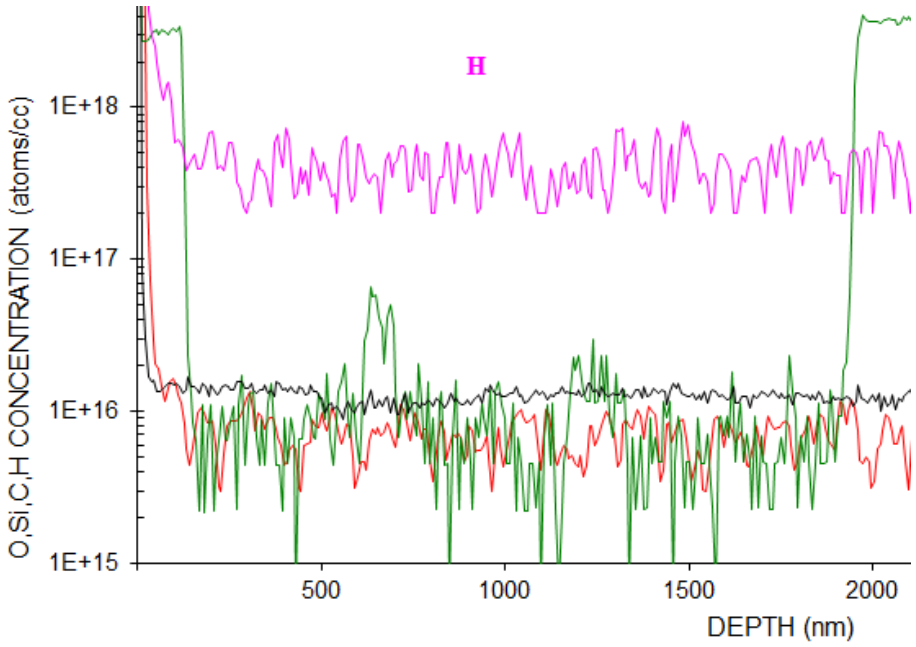
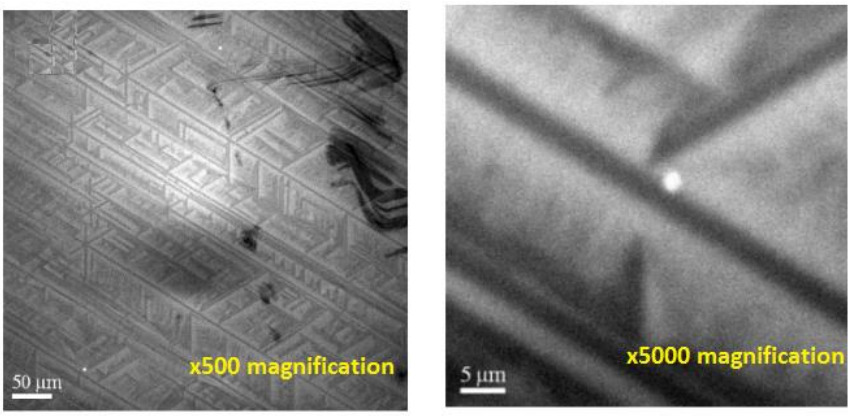


Figure 2.11: SIMS results for carbon incorporation unintentionally doped (u.i.d) in MOCVD GaN (Thomas Swan) as a function of growth rate and temperature.

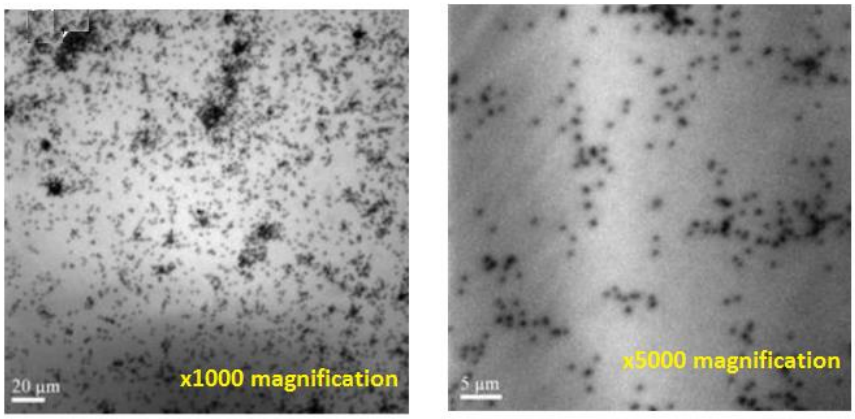
2.2.3 Issues with bulk GaN substrates

Since free-standing GaN substrates have still not been completely developed, the quality of substrates received varies with each shipment/batch, even from the same vendor. A number of different vendors (Furukawa, Kyma, Nanowin, Hitachi, etc.) were tried. Some wafers were good, but others from the same vendor had large visible defects and/or were completely non-uniform. Thus, each shipment had to be inspected via Atomic Force Microscopy (AFM) and Cathode Luminescence (CL) (CLs performed by Yuuki Enatsu) before use. Examples of un-

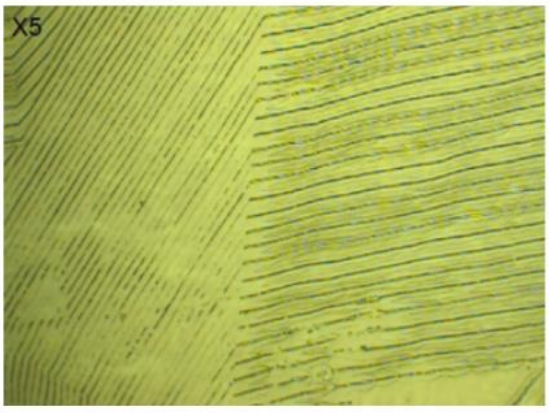
usable bare bulk GaN substrates are shown in figure 2.12. Some had large micro-cracks or pits, visible only under CL. Others had patterns visible even under an optical microscope.



(a) Large microcracks visible in CL



(b) High defect density visible in CL



(c) Features visible under microscope on a bare GaN wafer

Figure 2.12: Bare GaN substrates inspected in CL and under an optical microscope.

The Van der Pauw Hall test structure that was grown on sapphire substrates (figure 2.13) earlier was repeated on bulk GaN substrates. To prevent leakage though the pits, a 3.5 µm thick Iron (Fe) doped buffer layer was grown, much thicker than the usual 1 – 2 µm. Low n-type doped layers were grown on top of the buffer layer. The bare substrates were inspected under CL and the areas with micro-cracks was marked. The CL "map" was compared with the Hall measurement "map" (figures 2.14 and 2.15). As expected, the "bad" areas on the CL map (those with micro-cracks) corresponded to areas where ohmic contacts could not be achieved for Hall measurement. On the "good" areas, however, high electron mobility, above 1000 $cm^2/V.s$ was measured for most dies at a carrier concentration of ~ 5 x 10^{16} cm^{-3}. The highest measured mobility on our samples was 1060 $cm^2/V.s$. It must be noted that there were high levels of C incorporated in these layers as it was grown on MOCVD 4. The electron mobility would possibly be much higher without the additional ionized impurity scattering due to C.

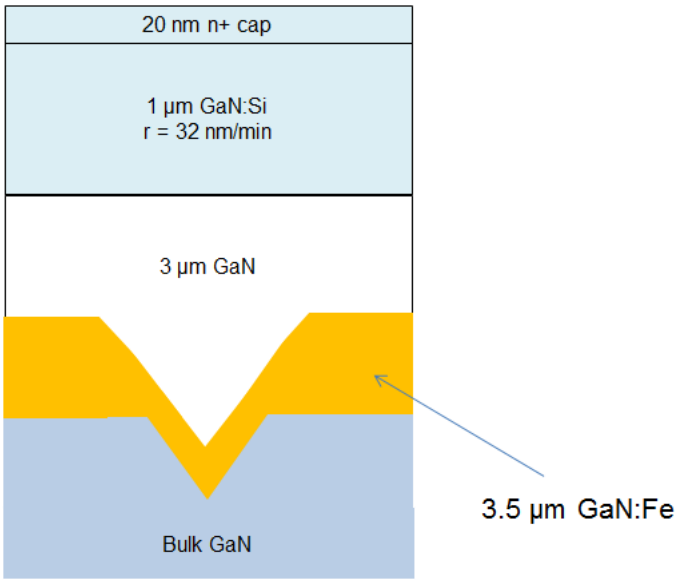


Figure 2.13: To avoid pit related leakage the thickness of the Fe doped layer was increased to 3.5 µm.

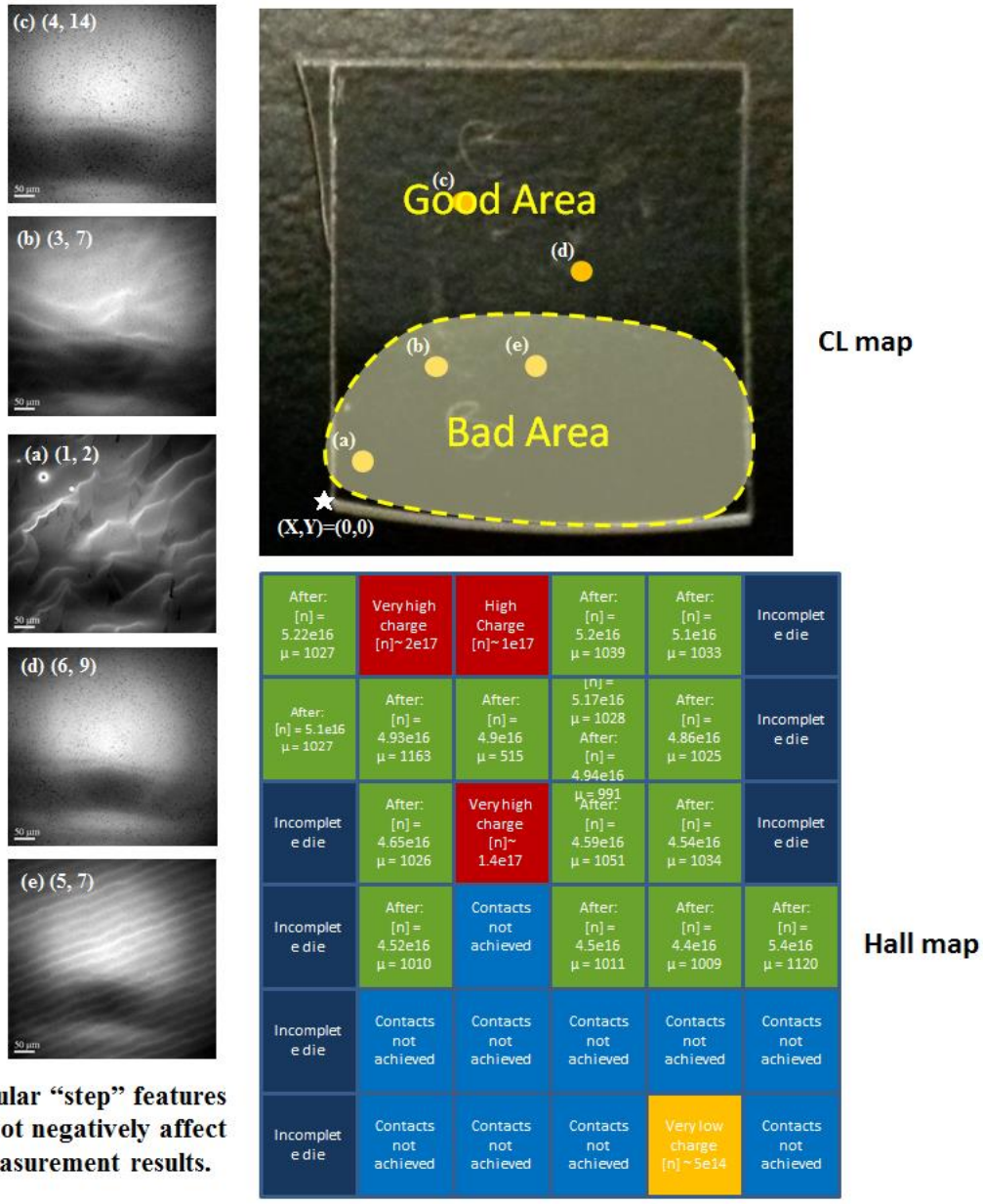


Figure 2.14: CL map marking good and bad areas of the bare GaN substrate piece compared with the Hall measurement map of the grown sample (structure given in figure 2.13). The green areas on the Hall map correspond to the "good" areas on the CL map.

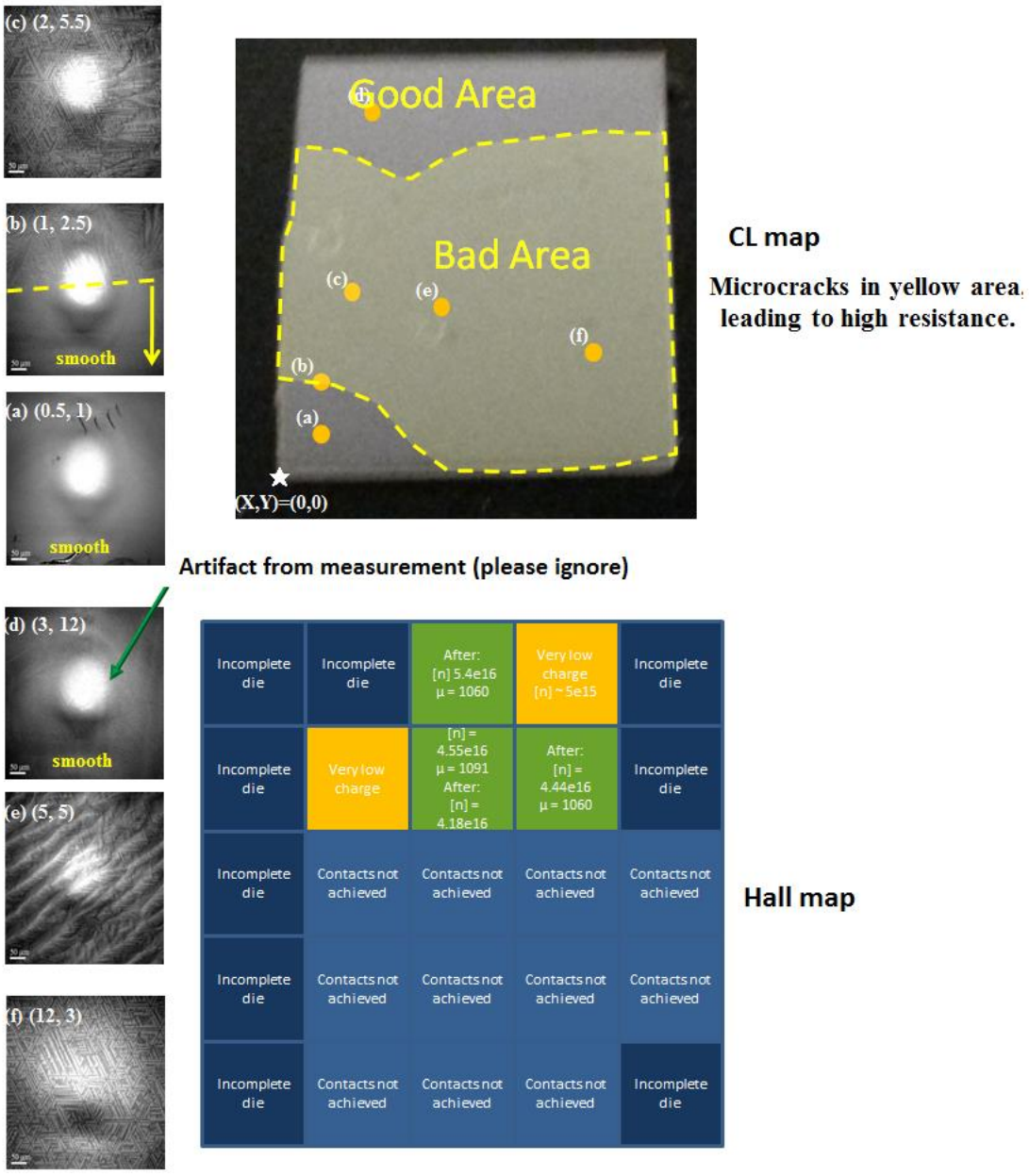


Figure 2.15: CL map marking good and bad areas of the bare GaN substrate piece compared with the Hall measurement map of the grown sample (structure given in figure 2.13). The green areas on the Hall map correspond to the "good" areas on the CL map.

2.2.4 Drift layers on bulk GaN substrates

The issue of carbon incorporation was solved by moving the GaN-on-GaN growth process to MOCVD 5 (Nippon Sanso) at UCSB. Capacitance-voltage (C-V) measurements were done on a test GaN-on-sapphire and a test bulk GaN piece prior to each full device growth to calibrate the doping on the given day. The n- type carrier concentration was extracted from the slope of the C-V plot using the following equation:

$$\frac{1}{C_{dep}{}^2} = \frac{2(\Phi_{bi}+V_r)}{qN\varepsilon_S A^2} \qquad 2.2$$

Where C_{dep} is the depletion-layer capacitance, Φ_{bi} is the built-in voltage, V_r is the applied voltage, N is the doping level, ε_s is the permittivity of the semiconductor (GaN in this case), and A is the area.

The test samples were confined in place (at the center) using corral wafers (typically 2" single-side polished sapphire wafers) cleaved to exact sizes. The test sample was kept in the center of the graphite holder as there is a growth rate gradient in both the MOCVD reactors. In MOCVD 5, it is better to grow in the center of the holder as the growth rates are very high on the edges, leading to insulating areas on the sample edges. The reverse is true in MOCVD 4, and it is preferable to tuck the sample to the edge ("lip") of the graphite susceptor.

Very good p-n diode breakdown voltage results were achieved on good bulk GaN substrates. The Si doping of the drift layers (typically 6 - 12 µm in thickness) was kept around 8 x 10^{15} cm^{-3} for the majority of samples. This was followed by 300 - 400 nm p-GaN doped with Mg doped at 3 x 10^{19} cm^{-3}, followed by 15 nm of p++ GaN:Mg doped at 1x 10^{20} cm^{-3}.

The full structure is given in figure fill and the I-V curve for a processed sample with this structure is given in figure 2.16. A breakdown voltage as high as 1100 V was obtained in some of the devices on this sample. The breakdown I-V curve is shown in figure 2.17.

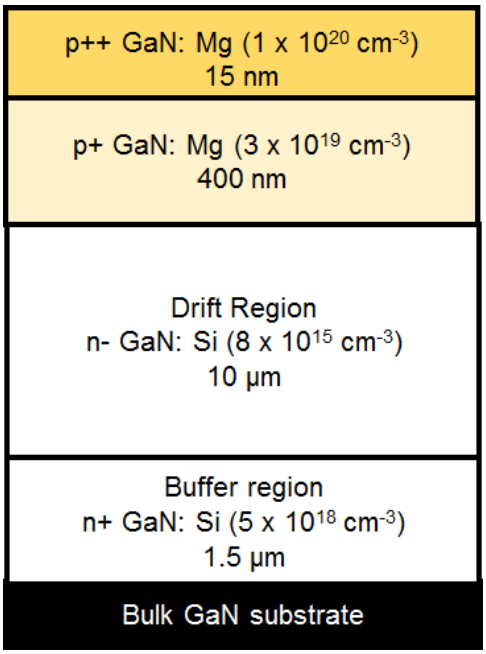


Figure 2.16: p-n diode structure grown on GaN substrates for breakdown measurements.

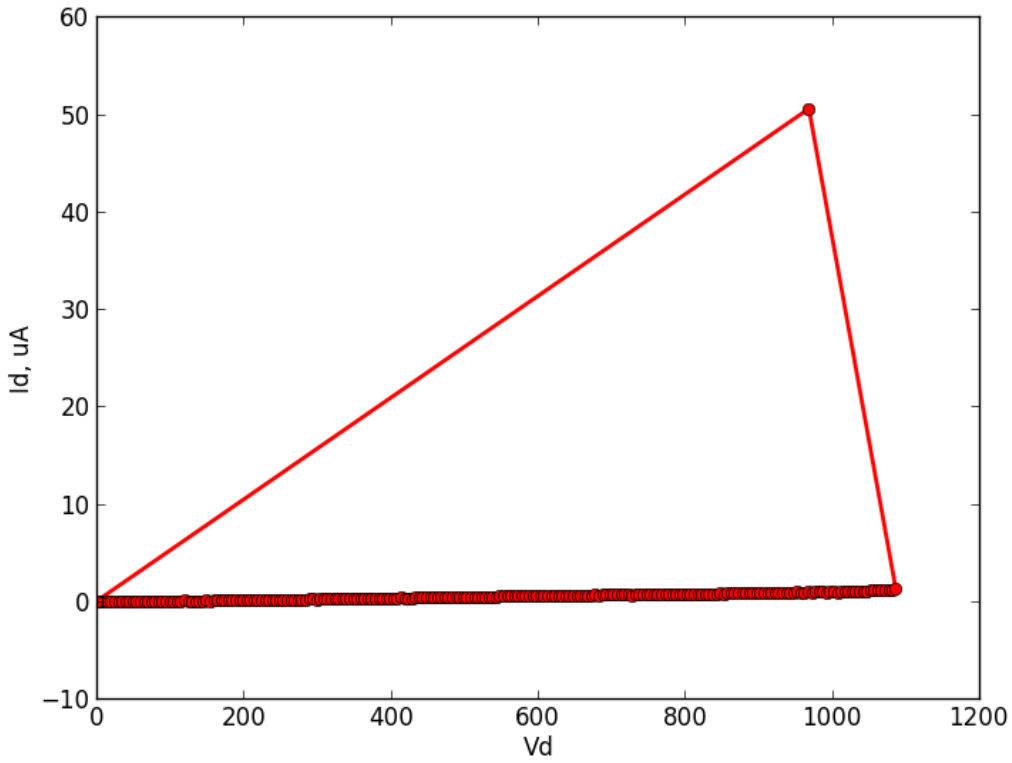


Figure 2.17: I_d - V_d characteristics of a p-n diode grown on GaN substrate with a 10 µm thick drift layer doped at Si: 8 x 10^{15} cm^{-3}. The full structure is given in figure 2.16. The V_{BR} for this device is about 1100 V.

2.3 Device Results

Our teams at UCSB and UC Davis fabricated and measured a number of different types of vertical GaN devices. Table 2-1 gives a summary of some of the best device results where the epitaxy was done by me.

Device	**Doping level (cm^{-3})**	**Thickness (µm)**	**Best V_{BR} (V)**	**R_{ON} (mΩ-cm^2)**
PN diode on sapphire	2 x 10^{15}	8	> 1000	N/A
PN diode on Bulk GaN	8 x 10^{15}	10	1100	N/A
OGFET	5 x 10^{16}	15	1400	2.2

Large Area OGFET	7×10^{15}	6	320	7.6
CAVET	8×10^{15}	6	450	16
Trench CAVET	5×10^{15}	15	880	2.7
MOSVFET	8×10^{15}	8	20	0.57

Table 2-1: Summary of device results

2.3.1 Oxide GaN-Interlayer Field Effect Transistor (OGFET)

The OGFET was first demonstrated on sapphire substrates, and led to a huge increase in I_{ON} from the addition of the GaN interlayer to a trench MOSFET. [18] The threshold voltage V_{TH} was 2 V, while V_{BR} was 195 V and R_{ON} was 3.8 $m\Omega.cm^2$. The DC characteristics significantly improved by using bulk GaN substrates instead of sapphire and incorporating a low damage gate trench etch (V_{TH} = 3 V, V_{BR} = 990 V and R_{ON} = 2.6 $m\Omega.cm^2$). [19] Further improvements were seen when MOCVD grown AlSiO was used as the gate dielectric instead of MOCVD grown Al_2O_3 (V_{TH} = 1.5 V, V_{BR} = 1200 V and R_{ON} = 2 $m\Omega.cm^2$). [20] Most recently, we demonstrated a V_{BR} > 1.4 kV by using a novel double field-plated geometry (V_{TH} = 4.7 V, V_{BR} = 1435 V and R_{ON} = 2.2 $m\Omega.cm^2$). [21] Figure 2.18 shows the cross-section of this device and figure 2.19 shows I-V characteristics and breakdown measurements.

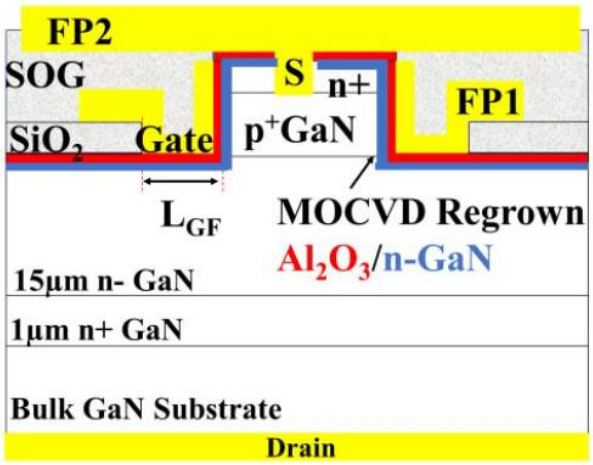


Figure 2.18: Schematic of the double field-plated OGFET with > 1.4 kV breakdown. [21]

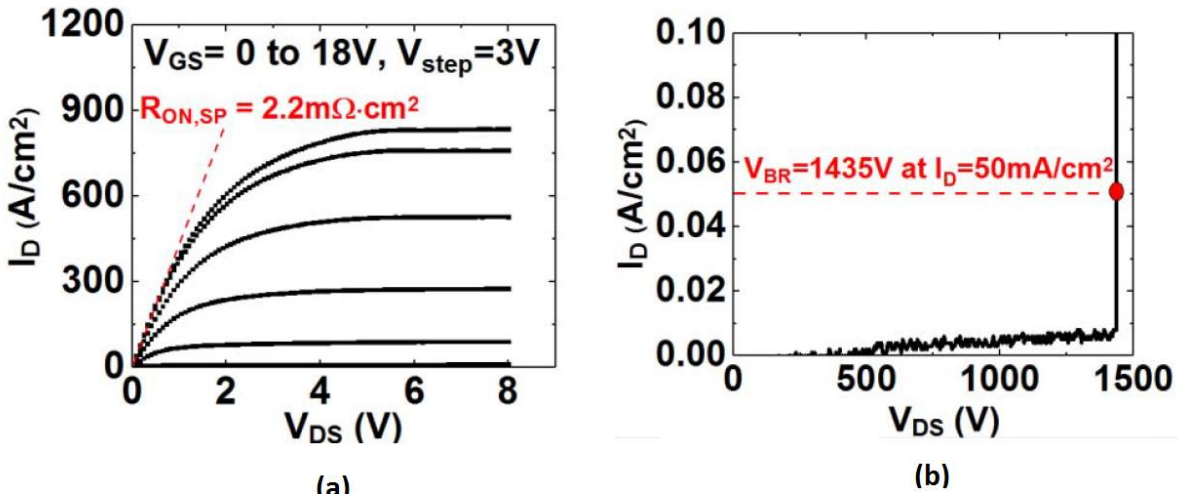


Figure 2.19: (a) I-V characteristics for a double field-plated OGFET [21] showing R_{ON} = 2.2 mΩ.cm^2 and (b) off-state characteristics showing V_{BR} = 1435 V.

2.3.2 Large area OGFETs

The OG-FET was scaled to 0.2 mm^2 to obtain a higher total current and subsequently, higher power. [22, 23] The scaled OGFET (figure 2.20(a)) demonstrated a V_{BR} = 320 V (figure 2.20(d)) and R_{ON} = 7.6 mΩ.cm^2 (figure 2.20(b)). For a single unit cell OGFET from in the

same sample, V_{BR} was as high as 700 V, measured at V_{GS} = −10 V (figure 2.20(c)). This corresponds to a breakdown electric field of 1.4 MV/cm and R_{ON} = 0.98 mΩ.cm^2. In another a large area OGFET sample grown on sapphire, a 1 A drain current was measured.

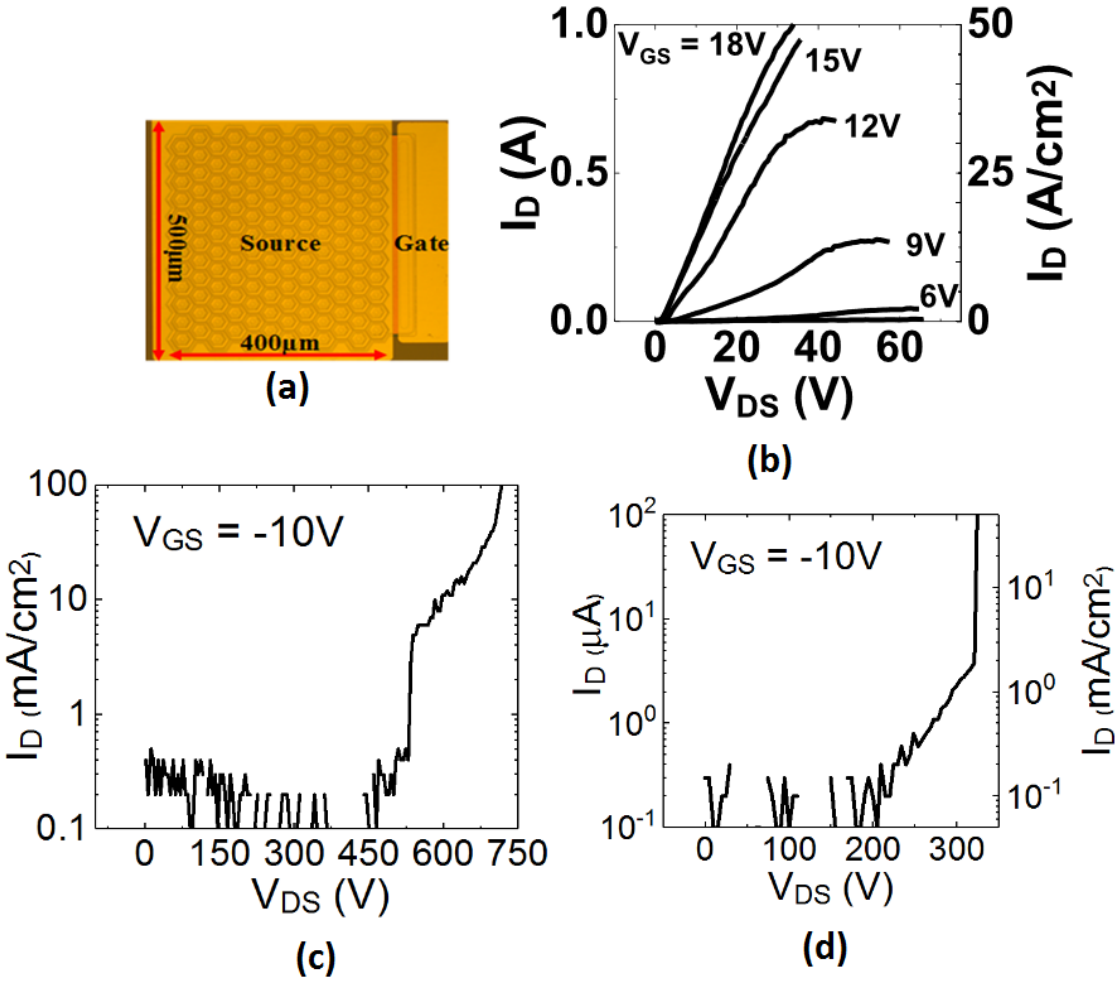


Figure 2.20: (a) Optical microscope picture of the scaled OGFET with an area of 400 µm × 500 µm on bulk GaN substrate. (b) I-V characteristics of the large area OG-FET on sapphire showing a drain current I_D as high as 1 A. (c) Off-state characteristics of a single unit cell OG-FET indicating a V_{BR} = 700 V and (d) of the scaled OG-FET indicating a V_{BR} = 320 V.

2.3.3 Current Aperture Vertical Electron Transistor (CAVET)

An n-channel CAVET (figure 2.21) was grown on a sapphire substrate using MOCVD. It had Mg-ion implanted Current Blocking Layers (CBLs) and a p-GaN gating structure. The channel was regrown using ammonia MBE. The p-GaN gated CAVET showed a significant improvement over current state-of-art AlGaN/GaN CAVETs with ion-implanted CBLs [15], both in terms of increased breakdown voltage of 450 V (figure 2.22), as well as reduced off-state leakage at a given bias. The pulsed I-V characteristics of the CAVETs showed no DC-RF dispersion under 5 μs pulse width (figure). [16]

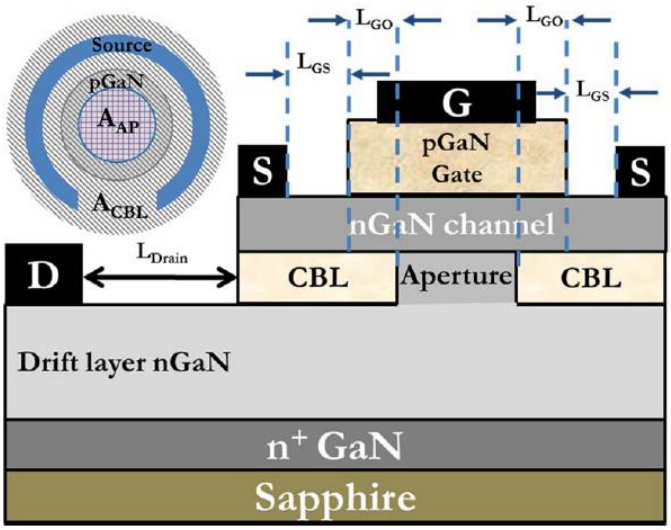


Figure 2.21: Device structure of the CAVET. Inset shows the top-view. Inner shaded area is the aperture and outer shaded area is the CBL. The p-GaN covers the entire aperture area. [16]

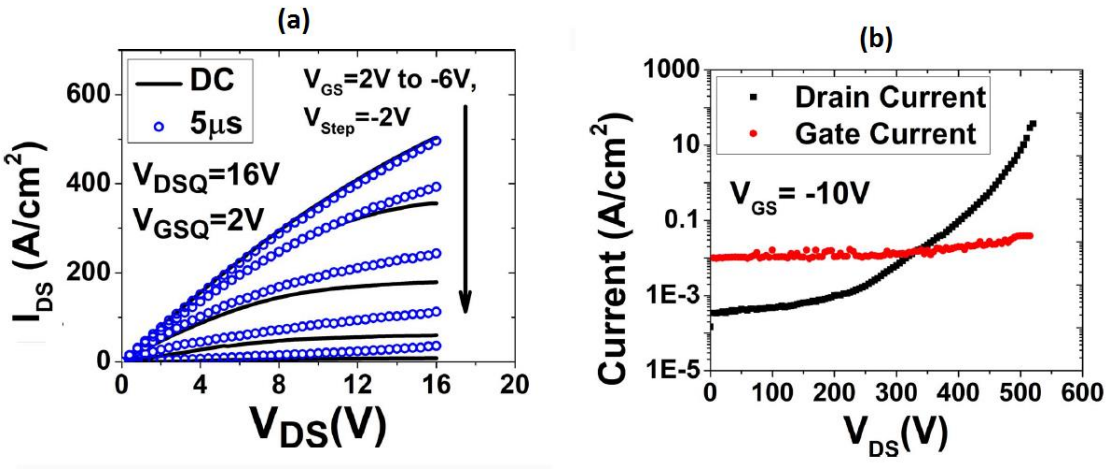


Figure 2.22: (a) Pulse I-V measurements show no RF-DC dispersion and (b) 3-terminal breakdown measurements give a 450 V breakdown. [16]

2.3.4 Trench CAVET

Dong Ji et al. [17] reported an MOCVD grown trench CAVET (figure 2.23) using with regrown AlGaN/GaN layers as the channel and in-situ Si_3N_4 as the gate dielectric. The device had a high V_{BR} of 880 V (figure) and a low R_{ON} of 2.7 mΩ.cm^2 (figure 2.24). A low hysteresis of 0.1 V was observed due to the high quality of the in situ Si_3N_4.

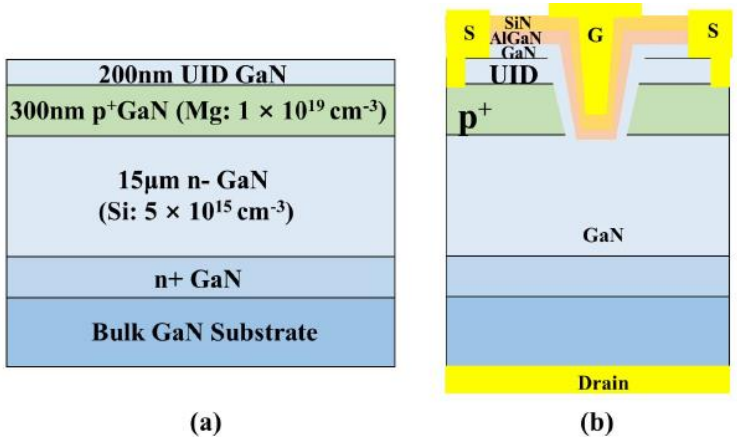


Figure 2.23: (a) Epitaxial layers for the trench CAVET grown via MOCVD (b) The full device structure. [17]

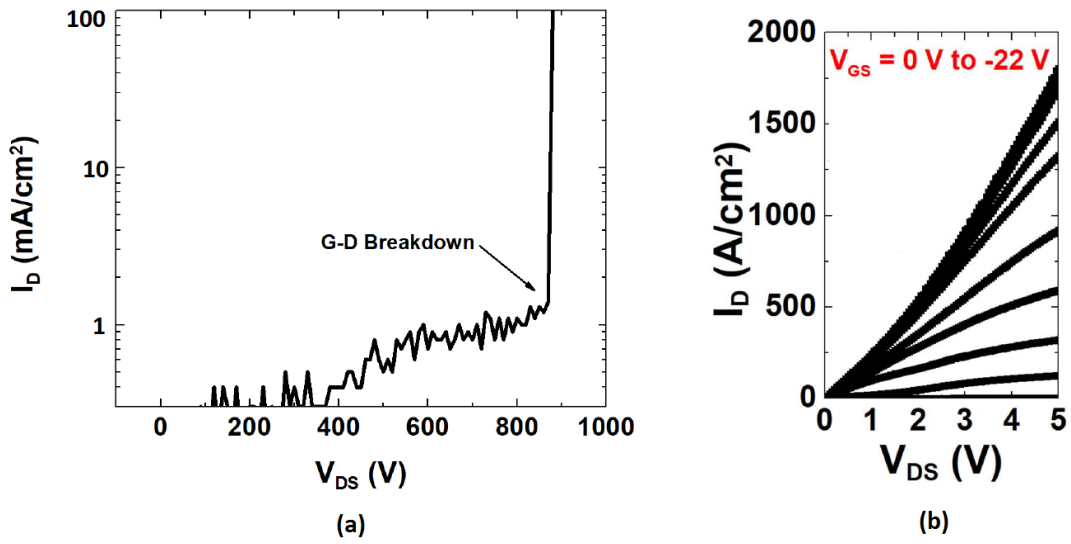


Figure 2.24: (a) The off-state breakdown voltage was 880 V, measured at V_{GS} = -30 V; (b) I-V characteristics of the fabricated trench CAVET show a low R_{ON} of 2.7 mΩ-cm^2. [17]

2.3.6 Vertical MOS-Gate Transistor (MOSVFET)

An excellent R_{on} of .57 mΩ.cm^2 was obtained in MOSVFET devices processed by Wenwen Li at UC Davis. [24] Figure 2.25 shows the I-V characteristics of one such sample. This device also delivered an output current of > 8 kA/cm^2. Much improvement is still required for such fin-MOSFET type devices (MOSVFET or VFinMOSFET), as the V_{BR} was low at 20 V, and it was normally ON (Vth = -13 V).

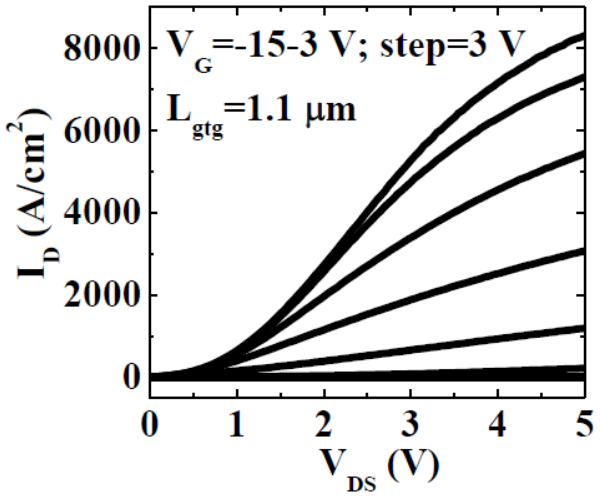


Figure 2.25: Output I_D-V_{DS} characteristics of the MOSVFET with R_{on} of .57 mΩ.cm^2 and an output current > 8 kA/cm^2. [24]

2.4 Conclusion

In this study, n-type carrier concentrations as low as 2 x 10^{15} cm^{-3} were obtained by careful optimization of the growth conditions on both, sapphire and GaN substrates. An electron mobility of ~ 900 cm^{2}V^{-1}s^{-1} was measured on sapphire samples with a doping of 1 to 2 x 10^{16} cm^{-3}. This is one of the highest ever reported electron mobility in GaN on sapphire. As this electron mobility was measured for electron transport perpendicular to the threading dislocations in the GaN films, higher values are expected for electron transport in vertical electronic devices. A high V_{BR} of 890 V was achieved for 6 μm thick drift layers with 2 x 10^{15} cm^{-3} doping and 640 V for 1 x 10^{16} cm^{-3} doping. The breakdown voltage for 8μm thick drift layers with 2 x 10^{15} cm^{-3} doping was greater than a 1000 V. On bulk GaN substrates, the highest measured breakdown voltage for a p-n diode was ~ 1100 V for drift layer thickness of 10 μm and doping of 2 x 10^{15} cm^{-3}.

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3 Inhibiting Magnesium Diffusion

Magnesium is most commonly used as p-type dopant for (Al, Ga, In)N films. In electronic devices, p-layer is usually sandwiched between adjacent n-type or u.i.d films. In the MOCVD process, surface riding causes Mg to propagate from p-nitride layers to subsequent n-nitride layers, compensating the n-type dopants, degrading the device quality, and complicating the fabrication process. Low temperature (LT) flow modulation epitaxy (FME) or "pulsed" growth was successfully used to prevent magnesium from MOCVD grown p-GaN:Mg layers from riding into subsequently deposited n-type layers. Mg concentration in the subsequent layers was lowered from ~ 1 x 10^{18} cm^{-3} for a medium temperature growth at 950 °C to ~ 1 x 10^{16} cm^{-3} for a low temperature growth at 700 °C via FME. The slope of the Mg concentration drop in the 700 °C FME sample was 20 nm/dec – the lowest ever demonstrated by MOCVD. For growth on Mg implanted GaN layers, the drop for a medium temperature regrowth at 950 °C was ~ 10 nm/dec compared to > 120 nm/dec for a high temperature regrowth at 1150°C. This drop-rate obtained at 950 °C or lower was maintained even when the growth temperature in the following layers was raised to 1150 °C. A controlled silicon doping series using LT FME was also demonstrated with the lowest and highest achieved doping levels being 5 x 10^{16} cm^{-3} and 6 x 10^{19} cm^{-3}, respectively. Further improvement in suppressing the surface riding of magnesium from p-GaN:Mg into subsequent layers was achieved via low temperature flow

modulation epitaxy. The slope of the Mg concentration drop was reduced to 3.5 nm/dec for a growth temperature of 620 °C – the lowest reported via MOCVD. The electrical quality of the top layer was verified by creating a 2DEG on top of the buried p-GaN layer, which exhibited a mobility of 1300 $cm^2 V^{-1} s^{-1}$. In addition, the FME layers were shown to block the Mg propagation more efficiently compared to sample in which an ex-situ wet etch was used.

3.1 Introduction

The most commonly used p-type dopant for (Al, Ga, In)N films is magnesium. In typical optoelectronic devices, the p-layer is the top layer of the device structure during growth. In electronic devices with p-layers, however, the p-(Al, Ga, In)N:Mg layer is often sandwiched between adjacent n-type or unintentionally doped (u.i.d) films. Examples of such GaN based electronic devices include bipolar transistors (HBTs) [1], CAVETs [2, 3] and trench MOSFETs [4]. Growing u.i.d. or n-type GaN layers on top of p-GaN layers doped with Mg has been a challenge for a long time. In the MOCVD process, Mg tends to propagate into subsequent layers due to surface riding [5-7], compensating the n-type dopants, and thus complicating the fabrication process of devices which require the deposition of Mg free layers on top of p-GaN:Mg. In the past this problem has been often circumvented by using Molecular Beam Epitaxy (MBE) for such layer stacks, where no Mg surface riding is observed, and slopes as steep as 2.5 nm/decade were measured at the interface between Mg doped and the un-doped top layer, most likely related to the significantly lower deposition temperatures [8]. Others methods to mitigate this issue include interrupting the growth after deposition of the p-GaN:Mg layer and removal of Mg from the surface by wet etching (slope 30 nm/decade) [6], inserting

AlN interlayers [9, 10] or GaN layers grown at reduced temperatures (slope 50 nm/decade) [6]. The insertion of an AlN layer is only applicable for applications which do not suffer from its presence, while using low temperature regrowth often leads to a deterioration of the structural properties of the layers, making these methods less attractive.

Another scenario where Mg propagation and redistribution plays a role is the regrowth on implanted Mg layers [11-13]. Mg doping by implantation is especially attractive for device structures where the presence of an Mg doped layer is required only in specific locations on the wafer, for example to block the current flow away from the aperture in CAVETs. Implanted Mg, however, is especially unstable [3], not only diffusing into regrown layers, but also redistributing in the preceding layers. These processes are less pronounced when the subsequent GaN layers are deposited at low temperatures. Flow Modulation Epitaxy or FME [14, 15] is a technique that modulates precursor flow between periods of growth and no growth. This kind of "pulsed" growth has been shown to enable the deposition of high quality layers at significantly reduced growth temperatures for GaN [16, 17]. If the regrowth can be performed successfully with N_2 as the carrier gas, then the passivation of Mg due to H_2 presence can also be suppressed [18]. This technique can be applied to both: growing Mg free layers directly onto the p-GaN grown inside the MOCVD reactor without taking out the wafer (in-situ), and also Mg implanted GaN layers. In addition to blocking Mg, it is important to be able to achieve a range of n-type concentration levels consistently. For example, a low 10^{16} n-type regrowth is preferred in the n-channels in CAVETs, while in most other devices, it is preferable to have as high a carrier concentration as possible to minimize the contact resistance [19]. Thus, low temperature regrowths should not only be effective in suppressing Mg surface riding, but also be tunable for different carrier concentrations.

3.2 Flow Modulation Epitaxy: Experimental discussion

3.2.1 FME growth conditions & Results

In the first set of experiments, 10nm thick n-type GaN FME layers were deposited onto semi-insulating (S.I.) GaN layers [20] to evaluate both, the surface morphology and the electrical properties of the layers. Typical full width at half maximum of the (0002) and $(20\bar{2}1)$ diffraction peaks of the S.I. GaN base layers amounted to 225 and 500 arcsec, respectively. All samples in this study were grown on sapphire substrates using TMGa, NH_3, ferrocene and disilane as precursors. The structure used for all these experiments is illustrated in figure 3.1(a). The top layer was 10 nm thick and was left unintentionally doped (u.i.d) for this initial optimization. Conditions explored included temperature, NH_3 flow, pressure, growth rate, N_2/H_2 admixture and the rest time between cycles. The surface morphology was inspected using a Dimension 3100 Nanoman AFM from Veeco. There was little to no morphological difference between the different parameters attempted other than temperature. While the surface of the FME layers grown at 700 °C resembled that of the underlying S.I. GaN base layer, the morphology started degrading at 675 °C (AFMs shown in figure 3.1(b)). Thus, 700 °C was used for all ensuing experiments. The conditions attempted, conditions used and the rationale for the choices are given in Table 3-1.

Growth parameter	Values attempted	Value used	Rationale
Temperature	650°C, 675°C, 700°C	700°C	Pit densities increased significantly at temperatures below 700°C
Ammonia flow	2 SLM and 6 SLM	6 SLM	Low C + O incorporation
Pressure	100 and 600 torr.	600 torr.	Low C incorporation
Growth rate	0.9 and 1.8 nm/min	0.9 nm/min	Low growth rate for low C
N_2/H_2 admixture	Grown completely in N_2 or H_2	Grown completely N_2	N_2 preferred to avoid Mg passivation

Rest time	3 secs and 12 secs	3 secs	Shorter rest times between cycles lead to reduced total growth time

Table 3-1: FME growth parameters explored during the initial characterization.

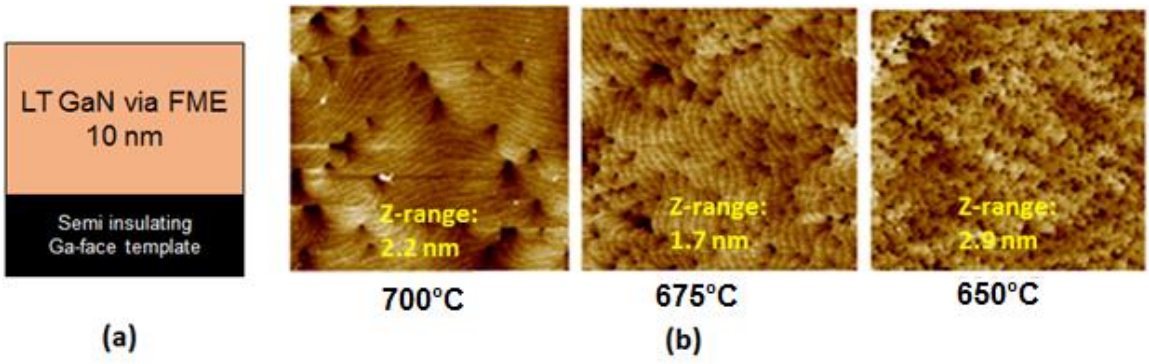


Figure 3.1: (a) Structure for the experiments optimizing growth conditions on a semi-insulating template (b) AFM scans of FME GaN layers grown at different temperatures. The pit density significantly increased at temperatures below 700 °C. All images are 2.5 µm x 2.5 µm in size.

3.2.2 Doping Series

Next, a series of Si doped FME layers was grown and characterized by Van der Pauw Hall measurements at room temperature. The purpose of this experiment was to see the minimum and maximum limits of n-type doping that could be achieved in GaN by the FME method using forementioned growth conditions. This would help determine the possible applications of this method; for example, low doping can be used for the aperture and channel regions of the CAVET, whereas very high doping levels could be used for contact regrowth on p-GaN:Mg. The thicknesses of the FME layers were 20 nm for doping levels above and 40 nm for doping levels below 6 x 10^{17} cm^{-3}. A linear trend in the carrier concentration versus Si dopant flow was observed as seen in figure 3.2(a). The structure used for this series was the same as figure

3.1, except that the top FME layer was Si-doped. A carrier concentration as low as 5 x 10^{16} cm^{-3} was reached with a low defect density. The highest doping level achieved was ~6 x 10^{19} cm^{-3}. The electron mobility was around 100-120 $cm^2/V^{-1}s^{-1}$ for most mid-concentration levels, but increased to 306 $cm^2/V^{-1}s^{-1}$ when the doping level decreased to 2.9 x 10^{17} cm^{-3}. At even lower Si doping, the electron mobility decreased again, most likely related due to insufficient screening of point defects in the FME layer. It was observed that the pit density significantly increased with increasing Si doping in the FME GaN layers (AFMs shown in figure 3.2(b)). [21] A similar trend was also observed for highly doped N-face GaN:Si layers deposited by MBE. [22] At the highest doping levels, three dimensional growth was observed, as reported in ref. 23. Nevertheless, since the very highly doped layers serve as contact layers, their poorer surface morphology does not negatively affect contact properties. The investigated doping range accommodates regrowth requirements for most device needs.

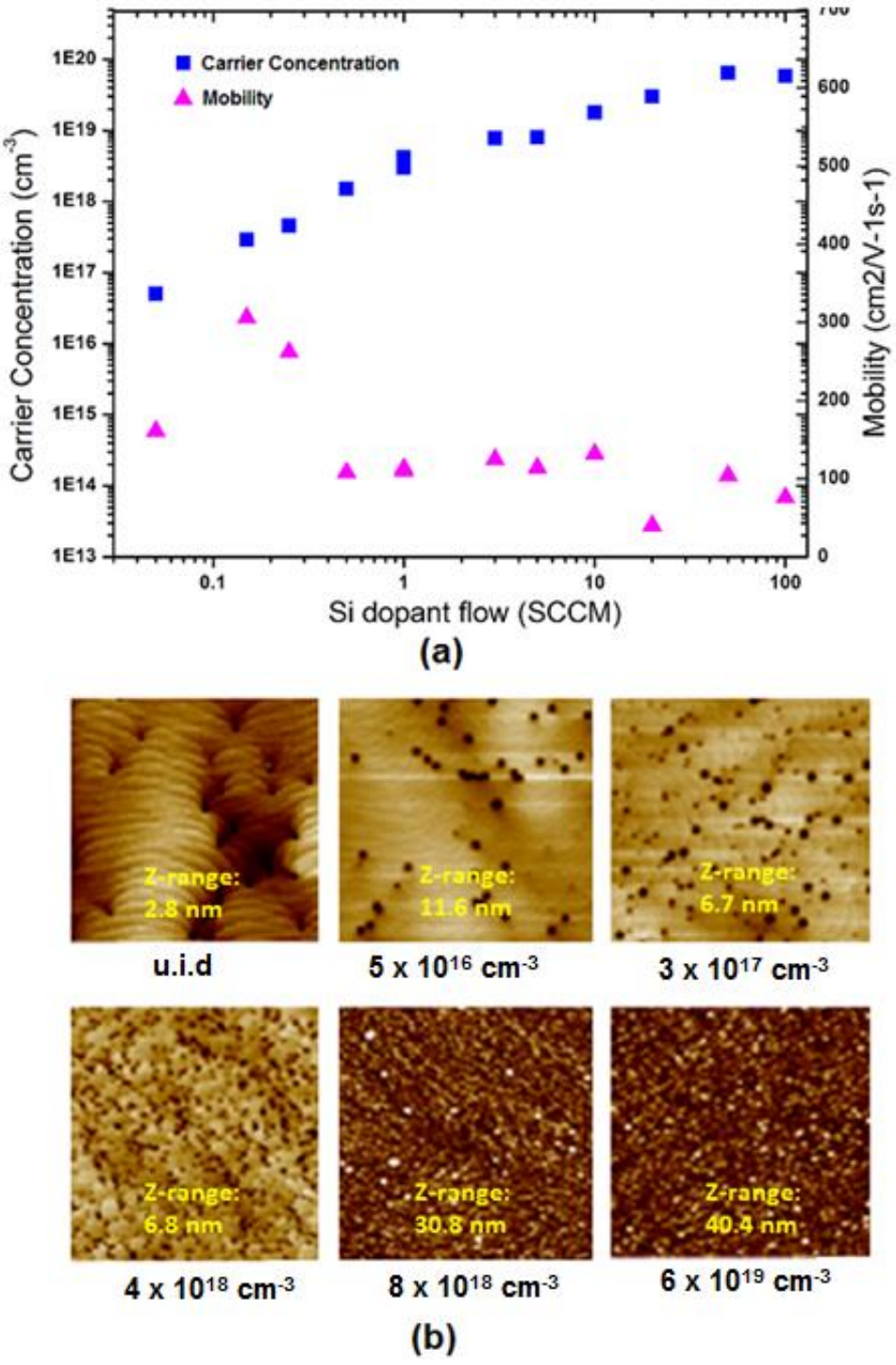
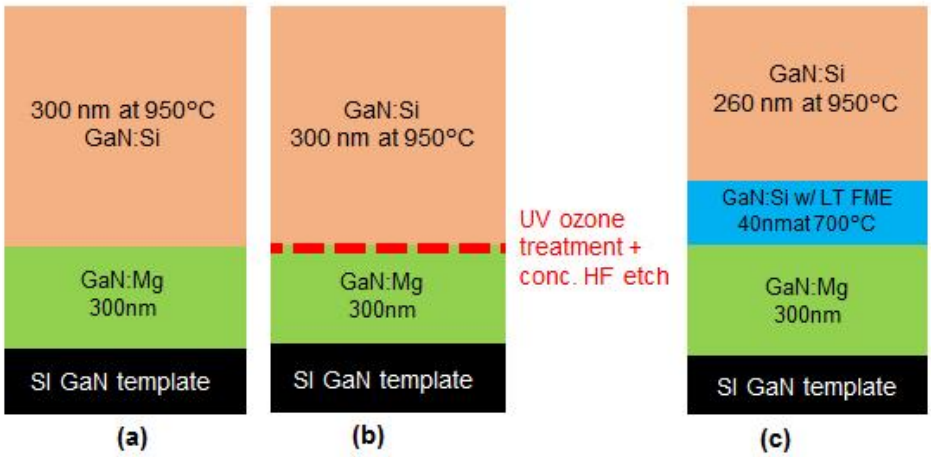


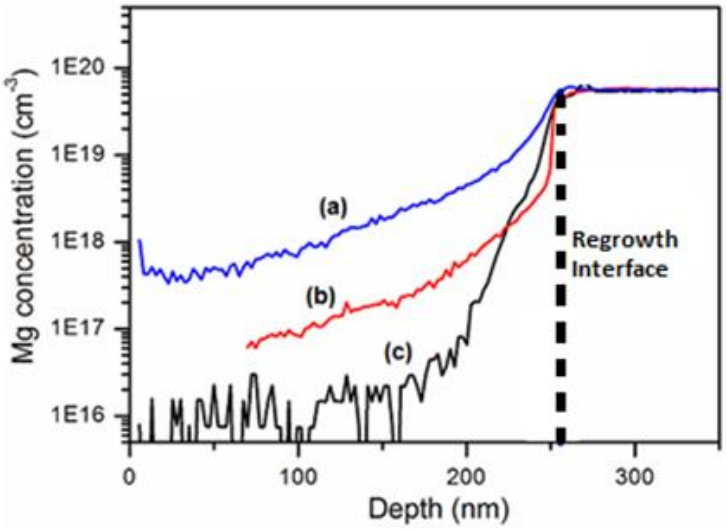
Figure 3.2: (a) Si dopant flow vs. the carrier concentration n and mobility μ (b) AFM images of GaN layers with different Si doping in order of increasing carrier concentration. All images are 2.5 μm x 2.5 μm in size.

3.3 Suppression of In-situ p-GaN:Mg

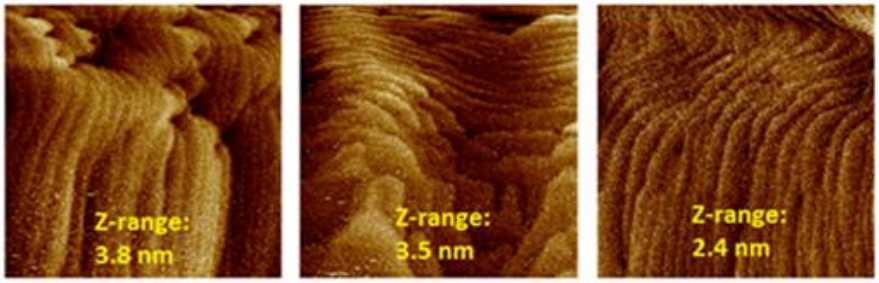
The optimized FME growth process was then used to grow n-type GaN directly onto p-GaN:Mg layers grown in-situ in the reactor, by first depositing a 40 nm thick GaN:Si layer by LT FME at 700 °C followed by a 260 nm GaN:Si layer grown in the conventional way at a medium temperature of 950 °C (figure 3.3(c)) The control samples consisted of in-situ p-GaN:Mg followed directly by 300 nm n-GaN grown at a 950 °C. There were two such samples: one was taken out of the reactor before n-type regrowth for a 2 minute concentrated HF etch (shown in figure 3.3(b)), while the other was grown in-situ (shown in figure 3.3(a)). The doping level in the GaN:Si layer was targeted to be ~ 3 x 10^{18} cm^{-3}. SIMS measurements were then performed with a Cameca IMS 7f Auto instrument. The SIMS Mg profile of the sample with the LT FME showed a sharp drop (20 nm/decade) as compared to > 80 nm/dec for the in-situ grown sample without FME GaN layer figure 3.3(d). This drop-rate is, to the best of our knowledge, the best yet reported for MOCVD. Xing et al. [6] demonstrated a drop rate of 30 nm/dec for their best sample, where the Mg surface layer was removed via wet etching prior to the ex-situ deposition of the GaN top layer. The LT FME sample in this study had a two orders of magnitude lower Mg concentration in the top layer ~1 x 10^{16} cm^{-3} compared to 1 x 10^{18} cm^{-3} Mg measured for the sample grown in-situ without LT GaN at a medium temperature of 950°C. For the third sample (in figure 3.3(d)), which was etched in concentrated HF prior to the ex-situ deposition of the medium temperature GaN layer at 950 °C, a one order of magnitude lower Mg concentration was observed, compared to the sample without an HF etch (figure 3.3(a)). This was, however, still one order of magnitude higher compared to the in-situ sample with the LT FME layer (figure 3.3(c)). This shows that low temperature regrowth was

more efficient than the surface Mg etch in suppressing Mg propagation for layers deposited on MOCVD grown p-GaN. The n-type carrier concentration determined by van der Pauw Hall measurements [24] in the top layer of the sample without LT FME layer and without the etch was 1.6 x 10^{18} cm^{-3}, while the concentration in the top layer of the sample with LT FME GaN was 2.5 x 10^{18} cm^{-3}, further proving the compensation effect of the riding Mg. The electron mobility for both samples was ~ 160 $cm^2V^{-1}s^{-1}$, which was similar to the mobility values achieved in the doping series discussed in the previous section. While V-defects formed in samples grown in N_2 as the carrier gas, the defects were eliminated when the structures were grown in H_2 as illustrated in the AFM images depicted in figure 3.4. The electron mobility measured in the top GaN:Si layer increased to 288 $cm^2V^{-1}s^{-1}$ for the H_2 grown sample at a doping level of 3 x 10^{18} cm^{-3}. All three test structures were smooth and had a low dislocation density, as seen from their AFM images displayed in figure 3.3(e). The results show that the developed low temperature FME procedure was effective in mitigating Mg propagation into subsequent layers while maintaining good structural properties of the GaN:Si top layers. In addition, FME and atomic layer epitaxy (ALE) growth schemes are known to suppress the C-impurity incorporation into epitaxial layers grow at low temperatures. SIMS measurements showed that the C concentration in the FME layers in this study was the same as in the high temperature GaN base layers, ~ 1 x 10^{17} cm^{-3}, corresponding to the detection limit in our tool. While this background C level is relatively high, it represents the upper limit of the C concentration in the FME layers. Note that previous experiments using low temperature GaN interlayers grown in the standard MOCVD growth mode also blocked the Mg propagation, but also resulted in poor structural and electrical properties of the top layers, further confirming that low growth temperatures are the main factor in suppressing Mg propagation.





(d)



Test structure (a) Test structure (b) Test structure (c)

(e)

Figure 3.3: Test structures for (a) samples without the LT FME layer, (b) with a concentrated Hydrofluoric Acid etch, and (c) with an LT FME layer. (d) Mg SIMS profile of the test structures (a-c). (e) AFMs of the test structures (a-c). [25]

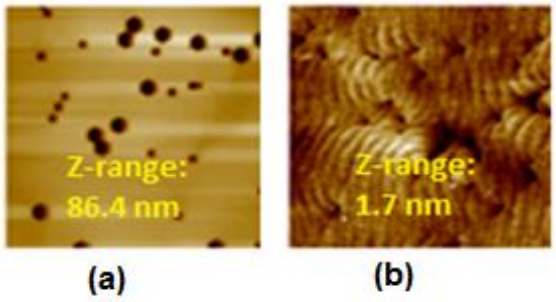


Figure 3.4: p-n regrowth with (a) N_2 as carrier gas and (b) H_2 as carrier gas. H_2 eliminated the V-defects formed during regrowth. All images are 2.5 µm x 2.5 µm in size.

3.4 Suppression of Implanted p-GaN:Mg

Similar experiments were repeated on implanted Mg test structures, as opposed to p-GaN grown by MOCVD. The Mg implantation was performed by Leonard Kroko Inc. at 80 keV. All samples underwent a solvent clean (DI water/Acetone/Isopropanol) followed by a 2 minute concentrated HF etch. The HF etch removes most of the Mg accumulated on the surface, as discussed before. Implanted Mg tends to more easily diffuse into adjacent layers compared to grown GaN:Mg layers. [11-13] Two structures incorporated the LT FME layer grown at 700°C, followed by conventional regrowth at 950 °C and 1150 °C respectively (figures 3.5(a) and (b)). The other two samples were grown directly at 950 °C and 1150 °C respectively with no LT FME GaN (figures 3.5(c) and (d)). The regrowth conditions used were the same as the in-situ p-GaN experiments. The Mg profile of all four test structures is displayed in figure 3.5(e), determined by SIMS. It is apparent that the only sample exhibiting elevated Mg levels in the

regrown layers was the one grown at 1150 °C. The drop-rate for this sample was ~ 250 nm/dec, as opposed to <10 nm/dec for all the other samples. Thus, one can conclude that any temperature at or below ~ 950 °C (medium temperature for GaN growth) results in a fairly sharp Mg profile. The redistribution of Mg on the backside of the implanted layer was similar in all samples. The Mg propagation into the GaN:Si top layers was again reflected in the electron concentration determined by Van der Pauw Hall measurements [24]. The electron concentration amounted to 7 x 10^{17} cm^{-3} for the sample with LT FME and a top layer growth temperature of 950 °C (figure 3.5(a)), 6.5 x 10^{17} cm^{-3} for the sample with LT FME and top layer growth temperature of 1150 °C (figure 3.5(b)), and 1.7 x 10^{18} cm^{-3} for the sample with no LT FME and top layer growth temperature of 950 °C (figure 3.5(c)). Most likely, the variations in the measured carrier concentrations between these 3 samples resulted from slight variations in the top layer thicknesses. The test sample with GaN:Si regrowth at 1150 °C only (test structure in figure 3.5(d)) was insulating, which can be explained by the SIMS result, revealing significant Mg propagation into the GaN:Si top layer. The AFM images for the samples are shown in figure 3.5(f). The surface of the sample grown completely at 950 °C looked significantly better than the one with inserted LT FME GaN layer. On the other hand, the surface of the sample with LT FME + 1150 °C grown GaN largely "recovered" due to the high temperature growth step, but some defect lines were still visible. Thus, the best overall properties were achieved using the medium temperature regrowths which successfully mitigated Mg propagation while still maintaining a good surface morphology. Comparing the regrowth results on etched MOCVD grown and implanted GaN:Mg layers, more abrupt Mg profiles were observed for the latter. The steeper slopes on the implanted samples were possibly associated with the lower Mg concentration on the surface of the implanted GaN:Mg

samples, which amounted to only 1 x 10^{19} cm^{-3}, as opposed to 5 x 10^{19} cm^{-3} for the MOCVD grown GaN:Mg layers. Further studies on samples with comparable Mg surface concentrations are needed to clarify this behavior.

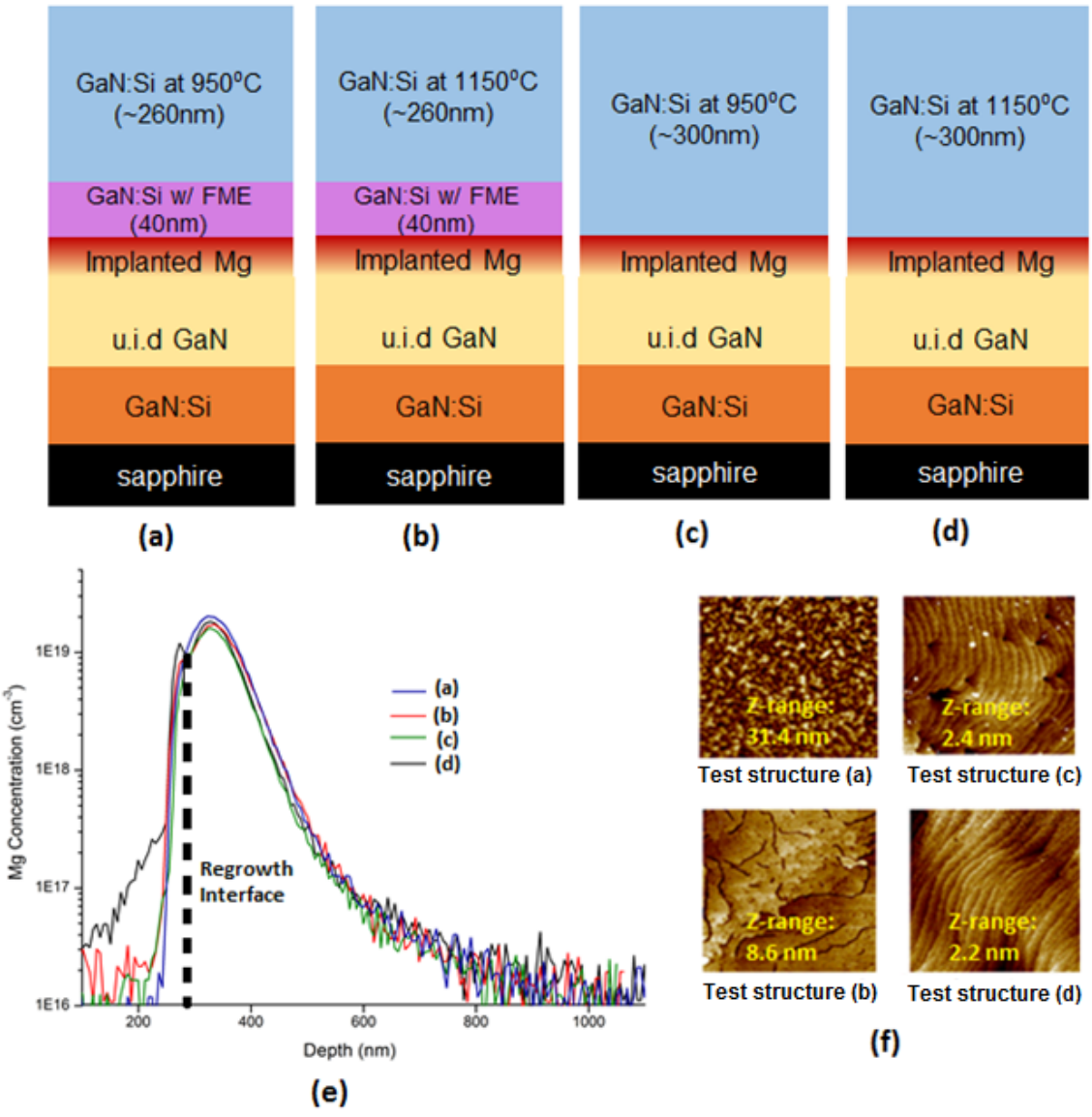


Figure 3.5: (a-d) Test structures for the experiment, (e) SIMS profile of the implanted Mg structures (a-d), and (f) AFMs of the implanted Mg test structures (a-d). All images are 2.5 µm x 2.5 µm in size.

3.5 Abrupt GaN/p-GaN:Mg junctions

MOCVD 5, which is the multi-holder Nippon Sanso at UCSB, has been used for all the experiments in section 3.5. The layer structure of the samples, as shown in figure 3.6(a), consisted of 300 nm of p-GaN:Mg grown at 1050 °C on top of a semi-insulting GaN template [20] using TMGa, Cp_2Mg, and NH_3 as precursors. This was followed by a 40 nm thick low temperature FME layers grown with TEGa at temperatures between 700 and 620 °C and finally a 250 nm thick layer grown at a medium temperatures of 900 – 950 °C with TMGa. Note that all given temperatures refer to the temperature of the heater and that the actual sample temperatures are about 100 degrees lower. The growth conditions for the FME layer included atmospheric pressure, 1.5 SLM NH_3 flow, 15 seconds of growth per growth cycle, 9 seconds of rest between cycles and a growth rate of 1.5 nm/minute. In the first set of experiments, the layers on top of the p-GaN were left unintentionally doped (u.i.d.). Secondary ion mass spectrometry (SIMS) measurements were performed on these samples to see the magnesium concentrations in each layer using the Cameca SIMS 7f Auto instrument.

Figure 3.6(b) illustrates the SIMS results obtained for p-GaN/FME GaN/ u.i.d GaN structures with FME layers grown at 620, 660, 700 °C. The deposition temperature of the u.i.d top layer was kept constant at 900 °C. The Mg drop rate decreased with decreasing FME layer growth temperature, and reached ~ 5 nm/dec for the 620 °C sample [33], a vast improvement from any previous result via MOCVD. The focused SIMS profile for the best drop rate (i.e. at 620 °C) is given in figure 3.6(c). This measured drop rate is also very close to the lowest reported value of 2.5 nm/dec for MBE grown p-GaN/u.i.d. GaN structures [24].

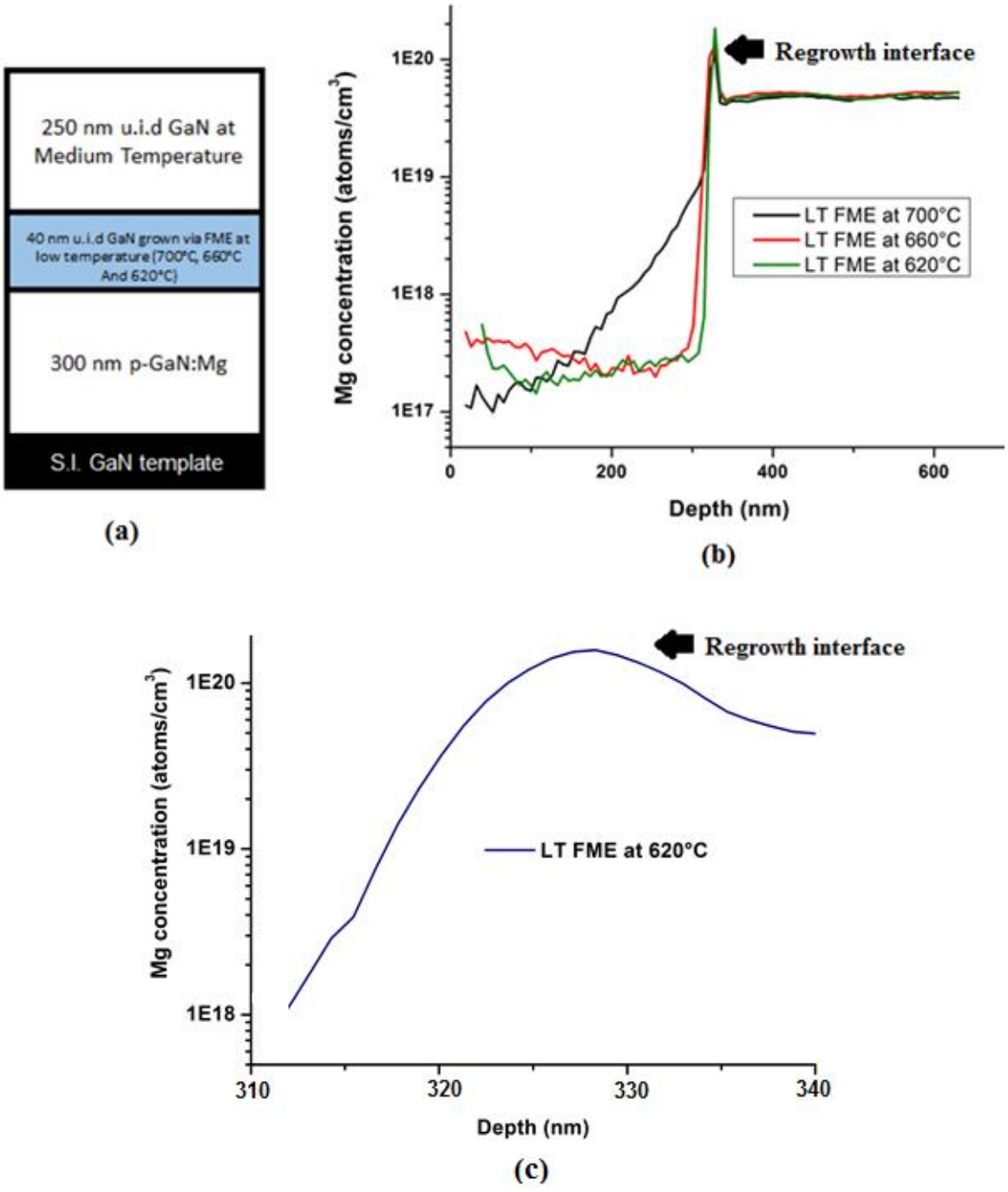


Figure 3.6: (a) Structure for the experiment testing different growth temperatures for the LT FME layer and (b) Mg SIMS profiles for the test samples (c) focused SIMS profile of the lowest Mg penetration condition, i.e. FME at 620 °C. An Mg drop rate pf ~ 5 nm/dec was achieved. [33]

Before reducing the top u.i.d. GaN layer growth temperature to 900 °C, like in the experiment above, the top layers were initially grown at 950 °C. At a FME layer deposition temperature of 660 °C but a top layer growth temperature of 950 °C, the residual Mg concentration in the GaN top layer amounted to 4 x 10^{17} cm^{-3}, a rather high value, whereas a top layer growth temperature of 900 °C resulted in a much lower concentration of 1-2 x 10^{17} cm^{-3}. This comparison can be seen in figure 3.7.

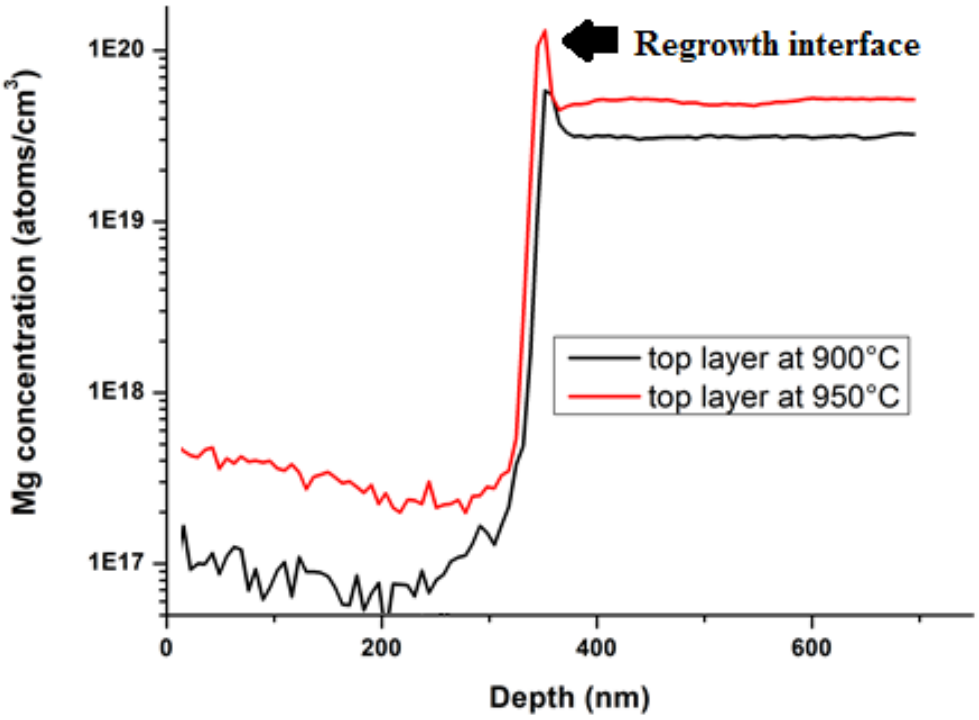


Figure 3.7: Mg SIMS profiles for samples with the top layer grown at 950 °C and 900 °C.

To further evaluate the properties of the layers grown on top of the GaN:Mg layers, a AlGaN/GaN heterostructure was grown on the stack instead of a single u.i.d GaN layer, as shown in figure 3.8(a). A control sample, which was a typical HEMT structure [29-31] without the p-GaN and the LT FME layers, was also grown for comparison, as illustrated in figure 3.8(b). For both samples, the $Al_{0.25}Ga_{0.75}N$ layer was 25 nm thick and grown at 980 °C. The

growth rate was 2.3 nm/min. TEGa, TMAl and NH_3 were used as precursors. The properties of the two-dimensional electron gas (2-DEG) at the AlGaN/GaN interface was studied by van der Pauw Hall measurements. The mobility of 1300 $cm^2 V^{-1} s^{-1}$ and sheet charge of 7.3 x 10^{12} cm^{-2} obtained for the structure with buried p-GaN:Mg were very close to the values of 1402 $cm^2 V^{-1} s^{-1}$ and 7.6 x 10^{12} cm^{-2} measured for the standard HEMT. This result implies that the magnesium concentration in the subsequent layers is low enough to not significantly influence the electrical properties of the 2DEG structure on top. This is required, for example, for CAVET like structures. [2, 3, 32]

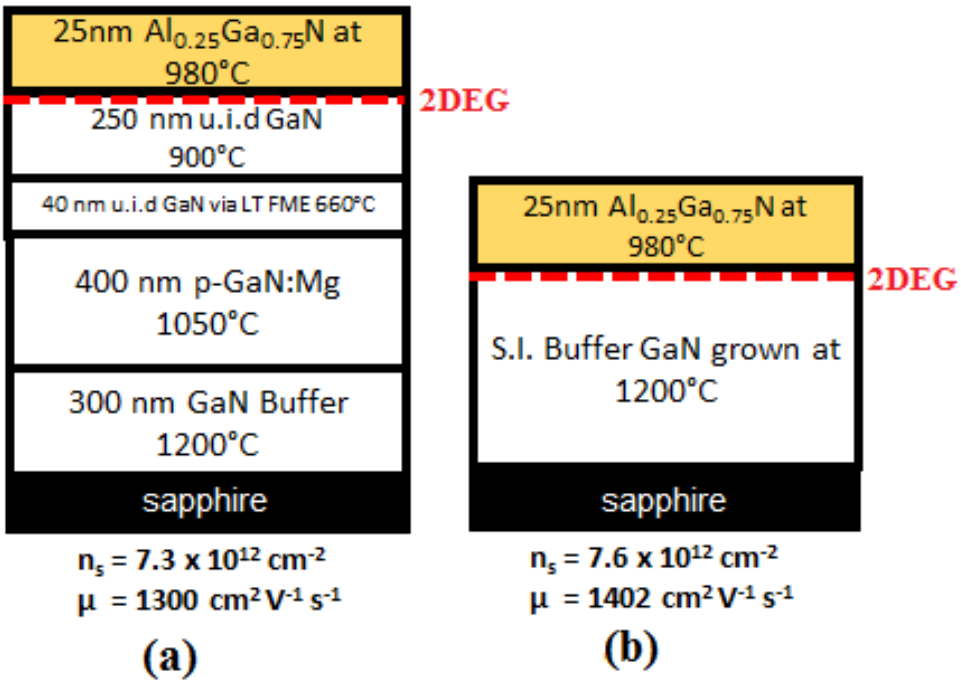


Figure 3.8: (a) AlGaN/GaN Heterojunction regrown on buried p-GaN versus (b) the control sample – a typical HEMT structure.

In a second experiment, 200 nm n^+ GaN:Si (n-type carrier concentration ~ 5 x 10^{18} cm^{-3}) layers were deposited at 1100 °C on top of low temperature FME layers (structure in figure

3.9(a)), and its sheet resistance was compared to another sample where the MOCVD growth was interrupted after the deposition of a 300 nm thick p-GaN layer and the Mg surface layer was removed by a concentrated HF wet etch (structure in figure 3.9(b)) [22, 32]. Afterwards the sample was re-loaded into the MOCVD chamber and the growth continued with the deposition at the GaN:Si layer. The layers were characterized by processing transmission line measurement pads on the samples. The sample using LT FME had a significantly lower sheet resistance (R_{sheet}) of 240 Ω/□ as compared to 500 Ω/□ for the wet etched sample. SIMS was performed on both samples (3.9(a) and 3.9(b)), and the results are shown in figure 3.9(c). The wet etched sample clearly shows higher Mg propagation and a much flatter slope that the sample that uses LT FME instead. The superior properties of the GaN:Si layer in the case of uninterrupted growth with FME layer confirm the results obtained in our previous study, which revealed a lower residual Mg content in layers grown on top if LT FME GaN compared to those where the deposition process was interrupted after GaN:Mg layer growth and the Mg on the layer surface was removed via ex-situ HF wet etch prior to the deposition of the top layer. These results support the use of a low temperature FME layer instead of wet etching for Mg propagation suppression.

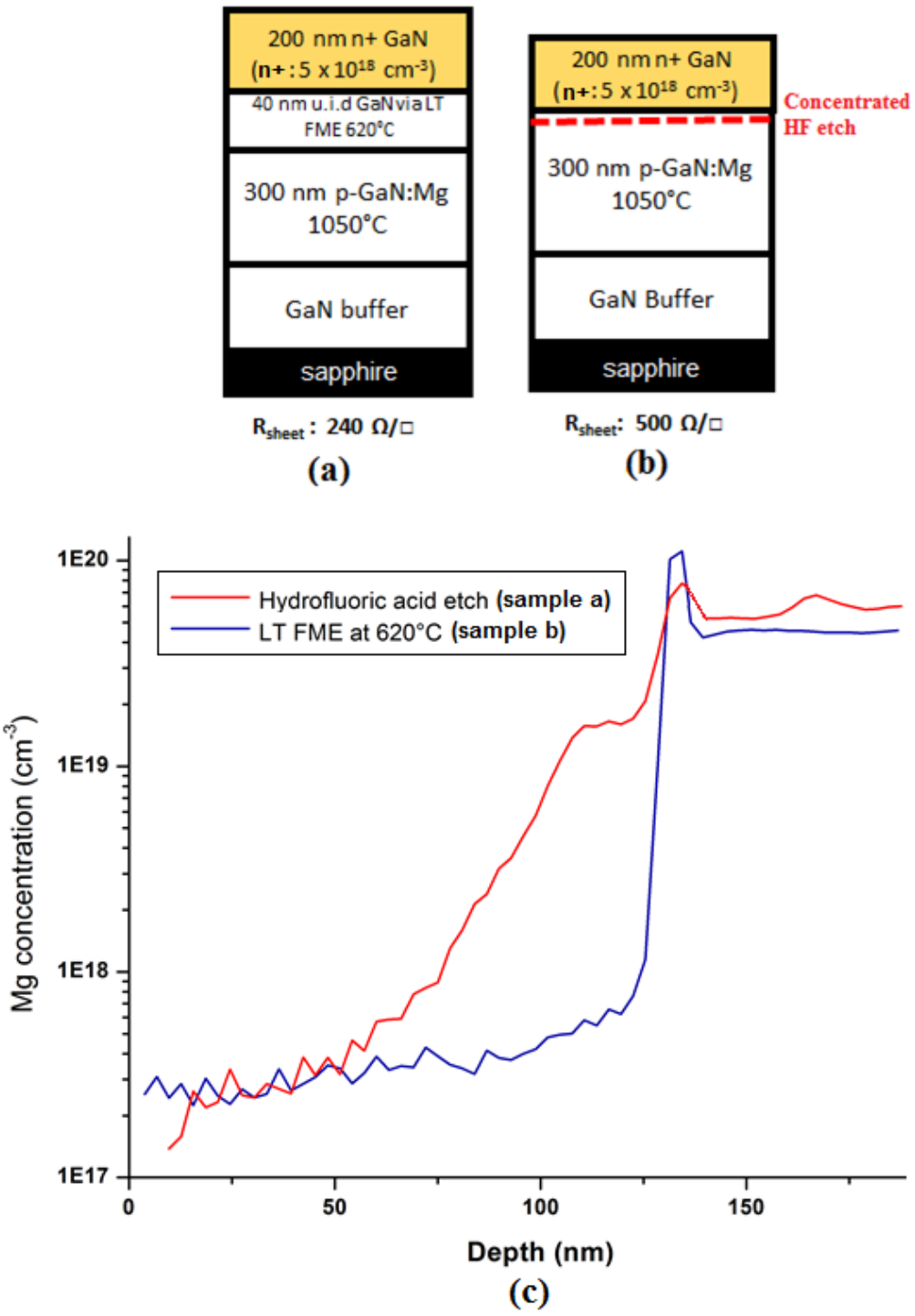


Figure 3.9: (a) Structure with LT FME layers for suppressing Mg versus (b) structure where a concentrated HF etch was to eliminate interfacial Mg. Plot (c) shows the SIMS measurement comparing the Mg concentrations in samples (a) and (b).

In summary, magnesium riding from p-GaN:Mg layers into subsequent layers was substantially reduced by lowering the growth temperatures in the subsequent layers. Lower temperatures typically tend to degrade the surface quality in the MOCVD process, but this issue was evaded by using a flow modulation epitaxy growth scheme. The Mg concentration drop rate was 5 nm/dec when the FME layer was deposited at 620 °C, a remarkable improvement from our earlier reported result of 20 nm/dec for regrowth at 700 °C, and values obtained by other techniques. These GaN/p-GaN junctions are comparable in abruptness to those obtained by MBE, where the lowest ever reported value was 2.5 nm/dec [24]. The magnesium concentration in the top layers could be further reduced from 4 x 10^{17} cm^{-3} to 1 x 10^{17} cm^{-3} by lowering the top layer growth temperature from 950 to 900 °C. The top layers were largely unaffected by the presence of the GaN:Mg underlayers, as substantiated by growing AlGaN/GaN heterostructures on top of the GaN:Mg layers. Transmission line measurements and SIMS confirmed that using LT FME led to better magnesium suppression than using a concentrated hydrofluoric acid etch on the interface.

3.6 Conclusion

In this work, low temperature (700°C) GaN growth with good morphology was deposited using FME. Controlled n-type doping between 5 x 10^{16} cm^{-3} and 6 x 10^{19} cm^{-3} was achieved in the FME layers. Mg penetration into following layers was successfully blocked on MOCVD grown p-GaN:Mg via low temperature FME regrowth with a drop-rate of 20 nm/decade, and continued to be blocked even when temperature was raised to 950 °C in the subsequent layers. Implanted Mg samples exhibited a sharp Mg drop in the regrown n-type

layers when the regrowth took place at a temperature of 950 °C or lower. This "medium" temperature range was found to be ideal for blocking Mg in implanted structures as further reducing the temperature did not lead to further suppression of Mg. Also, medium growth temperatures resulted in a better surface morphology than lower temperatures. Raising the temperature to 1150 °C once the Mg had been blocked by medium temperature growth did not lead to a rise in Mg levels, just like in the MOCVD grown p-GaN samples. This process will be very attractive for CAVETs which require implanted p-type layers followed by low concentration n-type layers. From a general perspective, the described technique can be applied to any device that requires highly doped contact layers on top of p-layers. Experiments implementing the FME process into devices are currently under way and the results will be presented in a forthcoming report.

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4 Regrowth in Ga-polar Trenches

The OGFET [1-5] (shown in figure 4.1) contains a thin GaN interlayer under the gate dielectric to enhance the electron mobility in the channel. This modification enables an increased current density and a lower on-resistance while maintaining enhancement-mode operation. The regrowth of the GaN interlayer has to be optimized such that the thickness of GaN grown on the sidewalls is similar to the bottom c-plane. The CAVET [6-11] (shown in figure 4.2), on the other hand, requires the complete filling of the aperture, which is surrounded by a current blocking layer. Non-planar filling of the aperture region could potentially increase the electric field under the gate and cause an early breakdown of this device [10], thereby impeding the full potential of the device design. An additional challenge for both types of devices is to block the magnesium from nearby p-GaN layers from diffusing into the regrown layers.[11] Colder growth temperatures have been shown to minimize Mg penetration.[12] While colder temperatures are useful for conformal growth (required in OGFETs), they are less attractive for CAVETs where high lateral growth rates are required to fill the trenches. Higher growth temperatures typically facilitate lateral growth. One potential solution could be to start growing at a lower temperature to block the surrounding magnesium, and then raise the temperature to fill the trench.

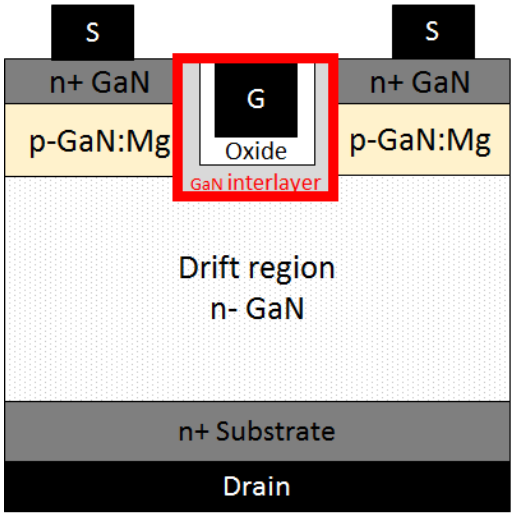

Figure 4.1: Schematic of the Oxide GaN-interlayer Field Effect Transistor (OGFET).[1-5] The GaN interlayer (marked in red) needs to be deposited under conditions which prevent Mg from the surrounding p-GaN from diffuse into the regrown layer.

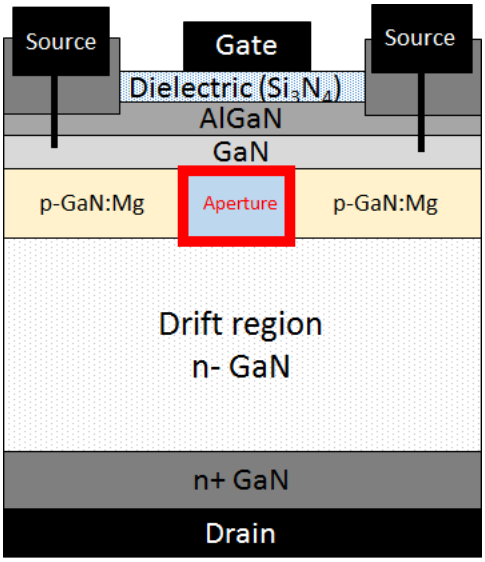

Figure 4.2: Schematic of Current Aperture Vertical Electron Transistor (CAVET).[6-11] The aperture (marked in red) should be completely filled while preventing Mg from the surrounding implanted p-GaN:Mg to diffusing into the aperture.

4.1 Experimental Design

For this study, blanket regrowth experiments were performed on GaN trenches with varying widths and optimized for two types of devices – those that required the profile of the trench to be maintained, and those that required the complete filling of trenches, i.e., a planar surface after regrowth. Low temperature $Al_{0.22}Ga_{0.78}N$ growth was optimized and used as the marker layer for SEM. GaN deposition at a medium temperature of 950 °C and using N_2 as carrier gas resulted primarily in growth on the (0001) plane, while the growth on the sidewalls was governed by the formation of slow growing semi-polar planes. This gave a conformal profile to the regrown GaN – useful for regrown GaN interlayer based vertical trench MOSFETs such as the OGFET. In contrast, high temperature (1150 °C) growth in H_2 resulted in high lateral growth rates. Planar surface was achieved under these conditions – a very promising result for CAVET-type devices.

4.2 Low Temperature AlGaN as marker layer

The first challenge in this study was to develop a marker layer to differentiate the regrown layers from the trench-etched base structure. This marker layer would not only have to be visible in the Scanning Electron Microscope (SEM), but also be of good crystalline quality. It would have to be deposited at a low temperature to follow the etched trench profile, as high temperatures can lead to a redistribution of GaN on patterned surfaces [13]. AlGaN was chosen for this purpose, as it is visible in the SEM and can sustain the high growth temperatures of subsequent layers. Thus, a growth process needed to be developed at a low temperature which

would give relatively good quality AlGaN. Trimethyl aluminum, trimethyl gallium and ammonia were used as precursors and about 15 nm of AlGaN was grown on Ga-polar GaN base layers under three different conditions (see figure 4.3(a)). Growth temperature, ammonia flow and composition of Al was varied, and a technique called flow modulation epitaxy (FME) or "pulsed" growth was used to obtain good morphology at such low temperatures [12]. The growth time per loop in the FME process was 26 secs and rest time was 3 secs. The growth rate was approximately 1 nm/min. In condition I, 2 SLM of ammonia was used for the growth, at a heater temperature of 700 °C, and the targeted Al% was 25%. Condition II was also at 700 °C and had an Al% of 25%, but used 6 SLM of ammonia. Condition III used 6 SLM of ammonia, a growth temperature of 800 °C, and an Al% of 22%. From the AFM images shown in figure 4.3(b), it was noted that good quality AlGaN layers were obtained when the Al composition did not exceed 22% and the FME growth temperature was 800 °C or higher. Surface steps were clearly visible for the sample grown using conditions III, and the electron mobility of the two dimensional electron gas, which formed at the AlGaN/GaN interface, amounted to 1161 $cm^2.V^{-1}.s^{-1}$ - a significantly higher value compared to those measured for the samples grown under conditions I and II. Thus, condition III was used for all marker layers in the ensuing studies, i.e. 22% Al, 800 °C and 6 SLM of ammonia. All temperatures in this paper refer to the heater temperatures, and not the substrate temperatures.

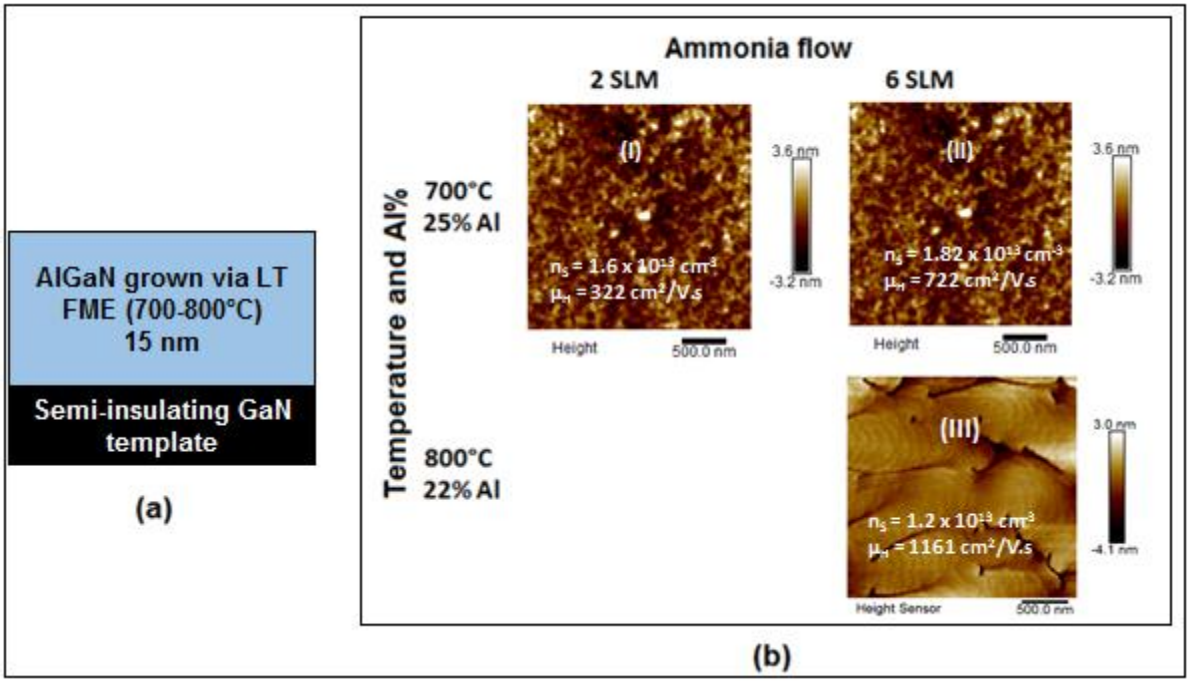

Figure 4.3: (a) test structure for the low temperature AlGaN series (b) AFM images of AlGaN layers grown by FME.[14] Surface Steps are visible at 800 °C (condition III) but not at 700 °C (condition I and II). Also shown are the results of Hall measurements performed on the same samples. The electron mobility was also significantly higher for samples grown under condition III.

4.3 Optimization of regrowth

For the actual regrowth series, 500 nm deep trenches of widths varying from 2 µm to 10 µm were etched into n-GaN templates (c-plane) using Reactive Ion Etching (RIE). The gases used were BCl_3/Cl_2, as BCl_3 removes oxides, while Cl_2 etches GaN. The etch was low power (15 W) to avoid surface damage due to bombardment of ions, with an etch rate of approximately 6 nm/min. The chamber pressure was 10 mTorr as low pressure increases the mean free path of the ions and promotes anisotropy. The photoresist was removed by an AZ NMP rinse (a 100% solution of N-Methyl-2-pyrrolidone (NMP) manufactured

by AZ Chemicals Inc.). This was followed by a concentrated hydrofluoric acid clean and DI water rinse. The mask used is shown in figure 4.5. Because the dry RIE resulted in semipolar sidewalls for both, m and a-planes, a wet etch using Tetramethylammonium hydroxide (TMAH) was attempted following RIE. TMAH etching often results in perfectly vertical sidewalls in GaN. In our samples, however, we obtained "shoe"-like corners for the a-plane sidewall, and a large deviation from the vertical plane of almost 60° for the m-plane sidewall (Focused Ion Beam (FIB) images shown in figure 4.4). All FIBs were performed by Onur Koksaldi.

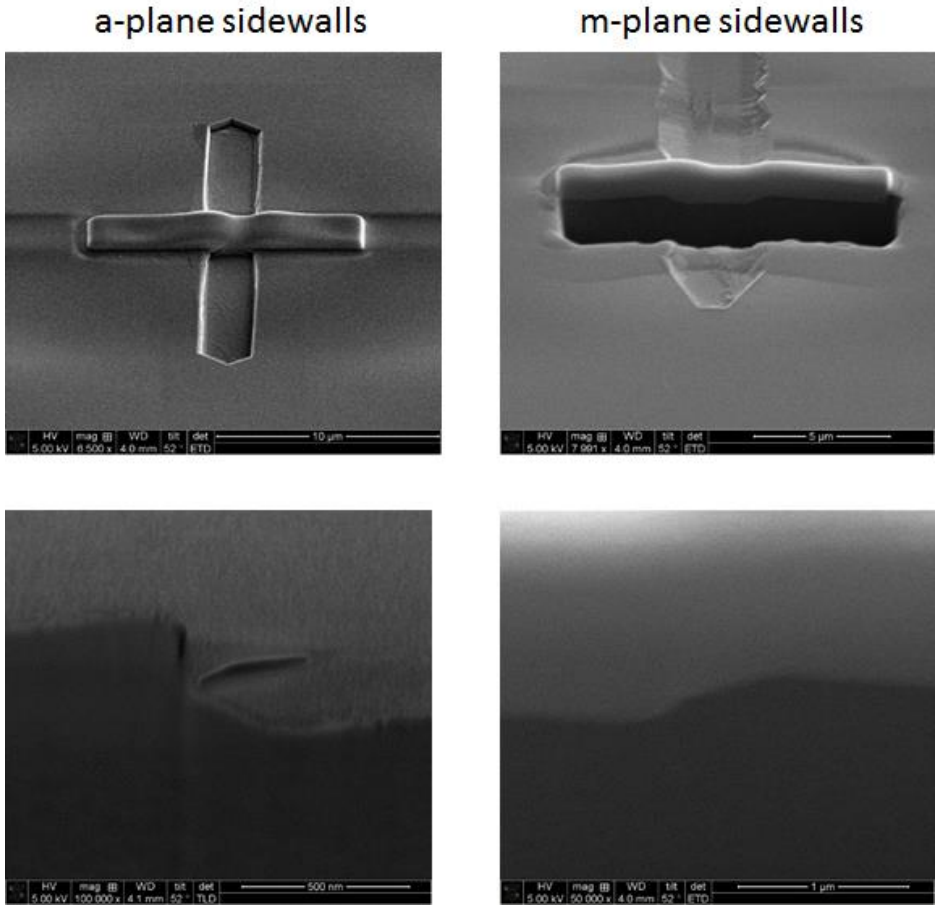

Figure 4.4: Cross-section of a-plane and m-plane trenches after RIE + TMAH etch.

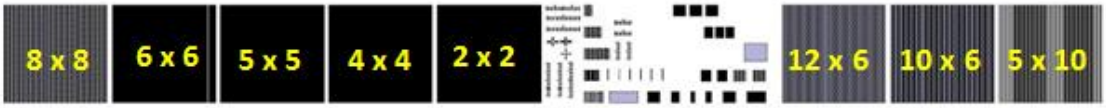

Figure 4.5: Mask with fin width – trench width combinations varying from 2 µm x 2 µm to 12 µm x 6 µm. The narrowest trench width was 2 µm and the widest was 10 µm.

The schematic of the cross-section of a sample trench is given in figure 4.6. First, a 5 nm thick interfacial GaN layer was grown via flow modulation epitaxy at a growth rate of 0.9 nm/min. This was followed by a 15 nm $Al_{0.22}Ga_{0.78}N$ marker layer deposited at 800 °C as described earlier. Finally, the 200 nm thick GaN layer of interest was grown at four different growth conditions (I-IV) as given in figure 4.7. Condition I and II were grown at a heater temperature of 950 °C and conditions III and IV were grown at a heater temperature of 1150 °C. A growth rate of 6 nm/min was used at 950 °C and 18 nm/min at 1150 °C. Conditions I and III used N_2 exclusively as the carrier gas, while II and IV used only H_2. Cross-sections of all samples were prepared using a Focused Ion Beam (FIB) and imaged via SEM. A medium growth temperature of 950 °C and N_2 as the carrier gas (condition I) lead to the formation of a semi-polar plane on the sidewalls. A high temperature of 1150 °C and H_2 as the carrier gas (condition IV) lead to higher lateral growth rates and almost filled the 2 µm wide trench completely except for a small kink in the center.

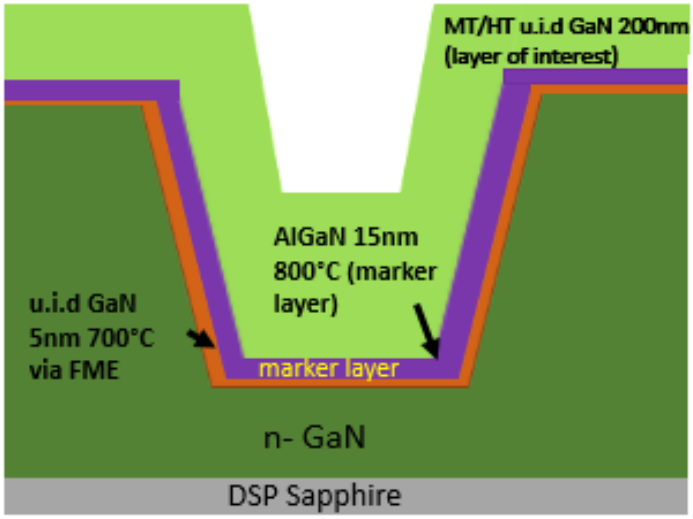

Figure 4.6: Schematic of the cross-section of a trench.

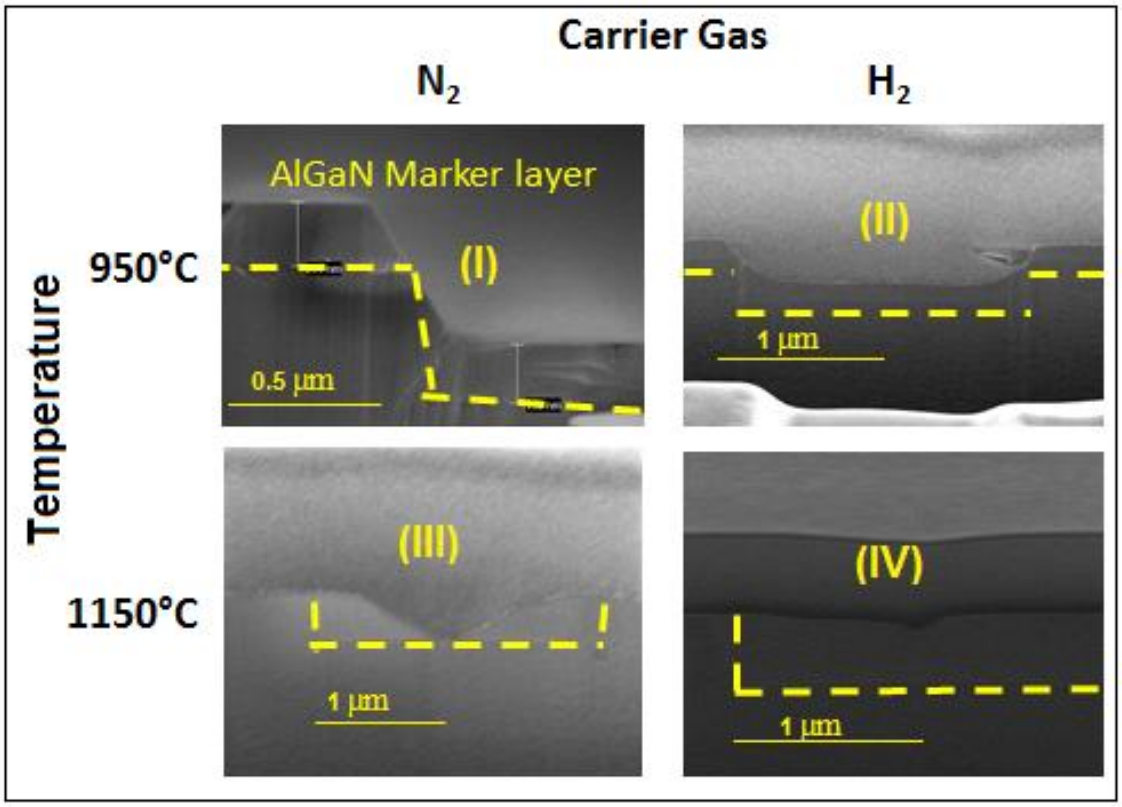

Figure 4.7: Results of the initial series.[14] High temperature and H_2 as carrier gas seemed to facilitate lateral growth rates (condition IV) while lower temperatures and N_2 initiated the formation of semi-polar planes

(condition I). The dashed yellow lines represent the AlGaN marker layers. They are clearly visible at a larger image size, but might not be clear to the reader at these sizes.

4.3.1 Filling of trenches

From figure 4.7, condition IV, it seems likely that just increasing the growth thickness slightly might result in the complete filling of the trench. But, as mentioned earlier, there is an additional challenge of blocking the magnesium from the surrounding p-GaN:Mg from penetrating into the regrown GaN while filling the trench for a CAVET aperture. Thus, 100 nm of medium temperature GaN was grown and followed by either 100 nm (condition I) or 200 nm (condition II) of high temperature GaN, as shown in figure 4.8. Condition II (100 nm at 950 °C + 200 nm at 1150 °C) filled up a 2 µm wide trench completely.

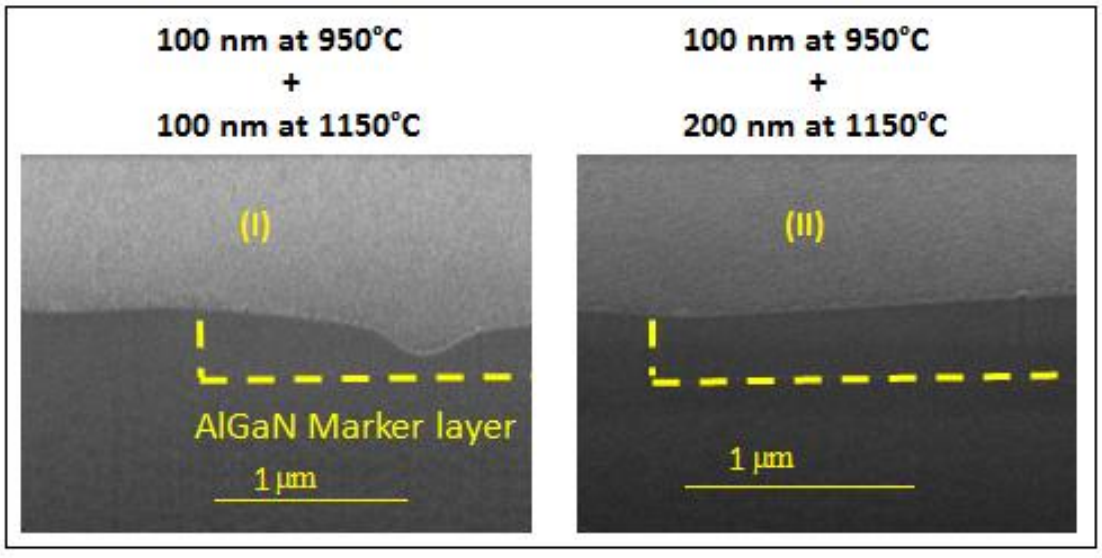

Figure 4.8: Optimization the growth conditions for trench filling: 100 nm of medium temperature (950 °C) GaN followed by 200 nm of high temperature (1150 °C) GaN regrown in H_2 leads to the complete filling of a 2

μm wide trench (condition II).[14] The dashed yellow lines represent the AlGaN marker layers. They are clearly visible at higher magnifications, but more difficult to see in these smaller images.

Secondary-ion Mass Spectroscopy (SIMS) was performed on a planar structure with similar regrown layers and a buried p-GaN:Mg layer underneath the regrown layers to mimic the current blocking p-layer in a CAVET. A concentrated HF clean was performed on the p-GaN:Mg surface prior to regrowth, identical to the HF clean performed after trench etching. The HF treatment is used to remove Mg which accumulated on the as-grown surface [12, 15]. The schematic layer structure for the SIMS experiment is depicted in figure 4.9(a). The results, shown in figure 4.9(b), indicate that the HF acid clean and the 100 nm medium temperature layer are successful in keeping the residual Mg concentration in the regrown layers at levels below 1×10^{17} cm^{-3}, dropping to values as low as 5×10^{16} cm^{-3} after 200 nm regrowth A similar result can be expected when regrowing in trenches, making this blanket trench filling regrowth technique attractive for CAVETs.

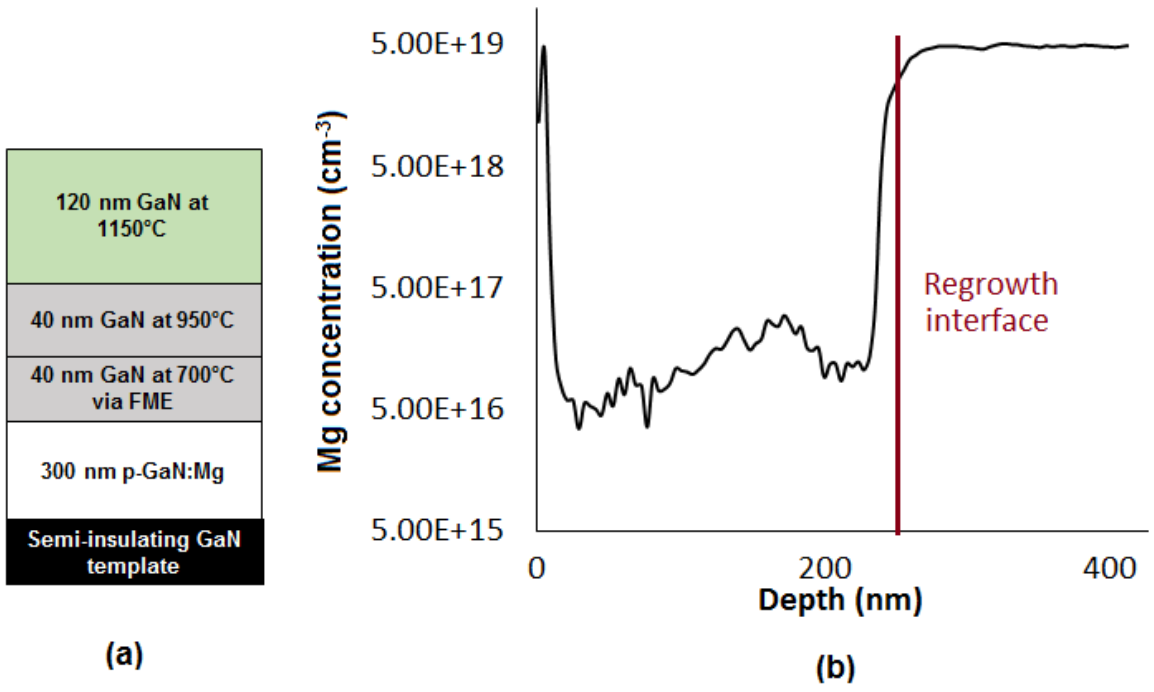

Figure 4.9: (a) Schematic sample structure with buried p-GaN:Mg for SIMS measurements (b) SIMS result [14] indicating that magnesium was largely prevented from penetrating into the top layers.

4.3.2 Conformal regrowth

Finally, conformal growth was explored by further dropping the growth temperature to 900 °C and using ammonia flows of 2 SLM (conditions I and III) and 6 SLM (conditions II and IV) as given in figure 4.10. The carrier gas was H_2 and the growth rate was 6 nm/min for all four conditions. The growth thickness was reduced to 100 nm to better match the requirements for thin GaN interlayers in OGFETs. Both, a-plane sidewalls and m-plane sidewalls were inspected. Using 6 SLM of ammonia (conditions II and IV), growth on both planes was conformal.

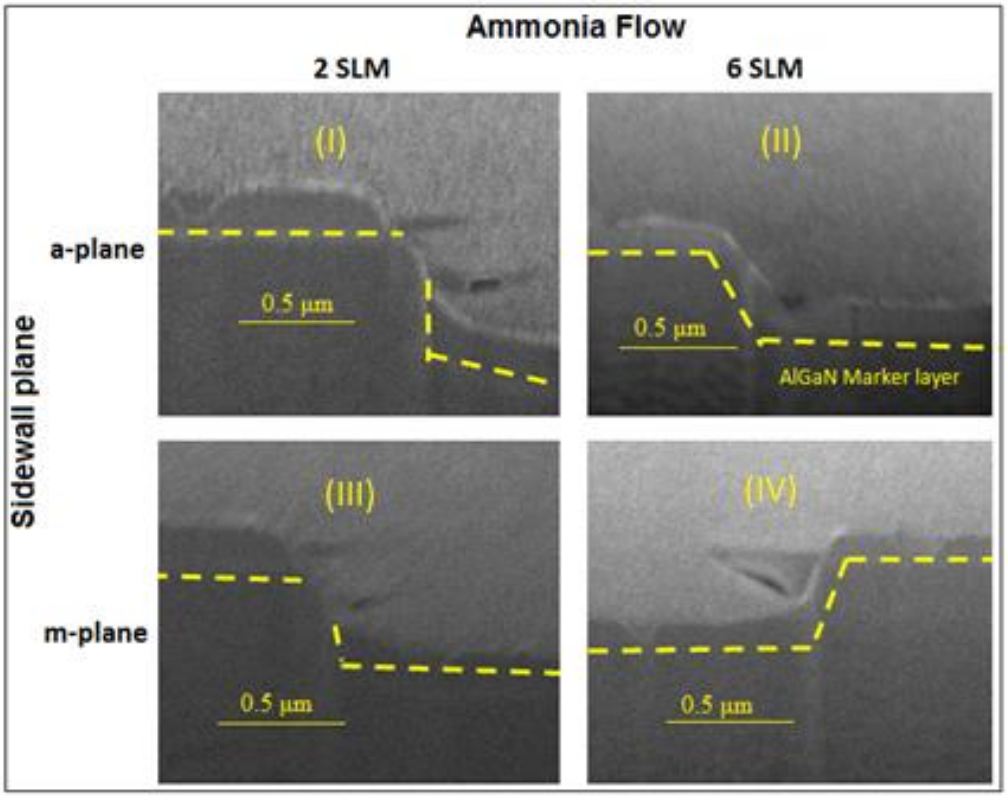

Figure 4.10: Optimization the condition for conformal growth. Growing at a medium temperature of 900 °C with 6 SLM of ammonia lead to highly conformal growth on both, a-plane and m-plane sidewalls (images II and IV, respectively).[14] The dashed yellow lines represent the AlGaN marker layers. They are clearly visible at higher magnifications, but more difficult to see in these smaller images.

4.4 Conclusion

Trench regrowth studies were performed on GaN-on-sapphire templates with 500 nm deep trenches etched by RIE, and widths ranging from 2 µm to 10 µm. GaN deposition at a medium temperature of 950 °C and using N_2 as carrier gas resulted primarily in growth on the (0001) plane, while the growth on the sidewalls was governed by the formation of slow growing semi-polar planes. Conformity was achieved for trenches with both a-plane and m-plane sidewalls at a deposition temperature of 900 °C and using a high NH_3 flow of 6 SLM. The latter

conditions are suitable for the GaN interlayer regrowth for OGFETs. In contrast, high temperature (1150°C) regrowth using H_2 as the carrier gas resulted in high lateral growth rates and complete trench filling - a very promising result for CAVET-type devices. Magnesium from the surrounding p-GaN:Mg could be blocked by initiating the regrowth at reduced temperatures followed by a higher temperature step to fill the trench, as confirmed by SIMS and nanoSIMS. From a general perspective, these results can be applied to any device that requires either trench filling, or conformity, without the use of masks. Using conditions similar to the ones above, conformal GaN growth was performed in-situ in an MOCVD along with the dielectric Al_2O_3 (done by Silvia Chan, graduate student at UCSB). Figure 4.11 shows the difference in on-current in a trench MOSFET device when a thin GaN interlayer was added – it increased from 125 A to 800 A at V_G = 15 V. [4]

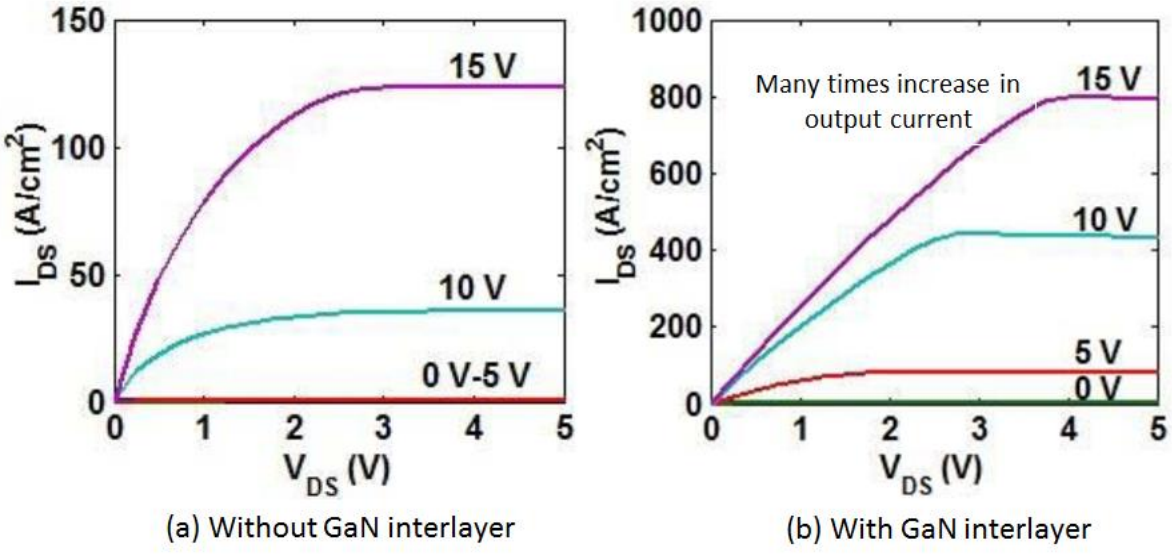

Figure 4.11: Comparison of the I_D-V_D characteristics of a trench MOSFET device without the GaN interlayer and with the GaN interlayer (OGFET) [4]. For the same gate voltage (15 V), the I_{ON} increased from 125 A to 800 A.

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5 Regrowth of AlGaN for N-Polar HEMTS

The need for extremely high frequency (30 – 300 GHz) transistors, also known as mm-band transistors, continues to grow. The wavelengths (λ) are in the 1 mm to 10 mm range. Earlier, this part of the spectrum was essentially unused simply because few electronic components could generate or receive millimeter waves. Mm-wave devices have made considerable progress in the last 15 years. They are now practical and affordable, and take the pressure off the lower frequencies in the expansion of wireless communication. The W-band part of the electromagnetic spectrum ranges from 75 to 110 GHz, and is used exhaustively for military applications such as satellite communications, millimeter-wave radar research, military radar targeting and tracking applications, and some non-military applications. GaN-based HEMTs are a leading technology for solid-state power amplifiers. Most reports for GaN transistors targeting W-band operation have been on devices grown in the traditional Ga-polar (0001) orientation [1-3]. While these devices have performed well, the N-polar (000-1) orientation provides several benefits to enable greatly improved performance. These benefits include the primary charge-inducing layer presenting a natural back-barrier displacing the 2DEG towards the gate electrode, and helping to provide a robust platform for forming low resistance regrown ohmic contacts. Furthermore, the inverted polarization in N-polar HEMTs allows a thin AlGaN cap to be added above the channel with an electric field that opposes gate

leakage. The N-polar orientation also enables a novel structure [4, 5] to reliably mitigate the DC-RF dispersion that often hinders mm-wave performance. This is achieved by adding a u.i.d GaN cap layer in the device access regions of the HEMT in-situ during device growth which replaces traditional ex-situ SiN_x passivation. This GaN cap also reduces surface depletion of the channel in the access regions leading to a reduction in access region sheet resistance. A typical N-polar deep recessed (NPDR) HEMT structure is given in figure 5.1. Romanczyk et al.[6] have recently demonstrated record power-added efficiency (PAE) of 27.8% while maintaining an output power density of 3 W/mm and 7.4 dB peak gain at 94 GHz.

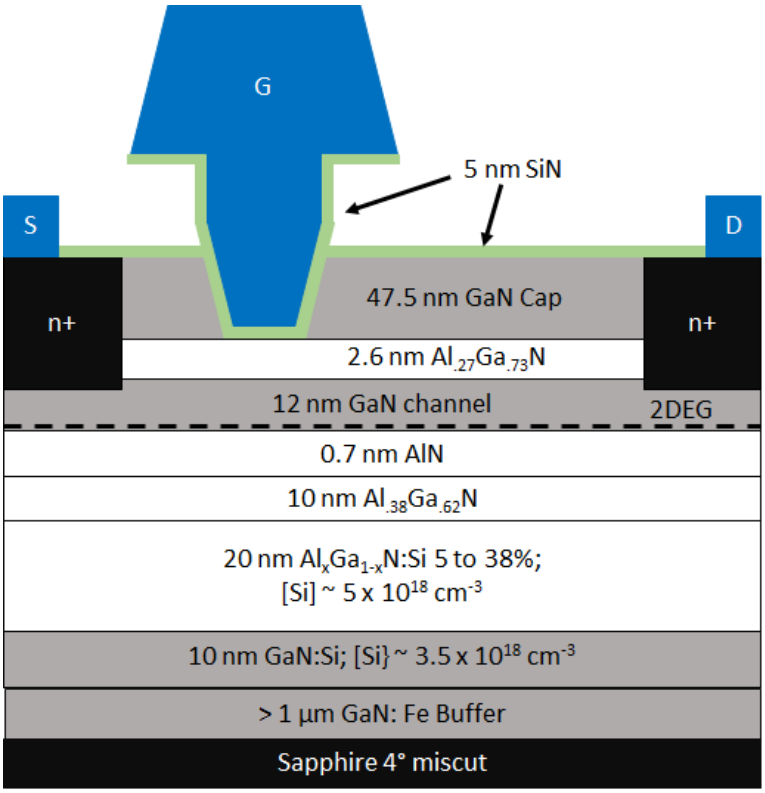

Figure 5.1. Device cross-section schematic highlighting key features of the N-polar GaN structure on a miscut sapphire substrate. [6]

An issue in the NPDR HEMT is the presence of the parasitic 2-DEG at the GaN cap/AlGaN cap interface, leading to lower breakdown voltages compared to a planar HEMT. Thus, there is a need to improve the V_{BR} in these devices. Since the deep recess breakdown occurs at the sidewall, it is proposed than a 2 – 3 nm thick high composition AlGaN cap layer can lead to a higher breakdown. The proposed structure is given in figure 5.2.

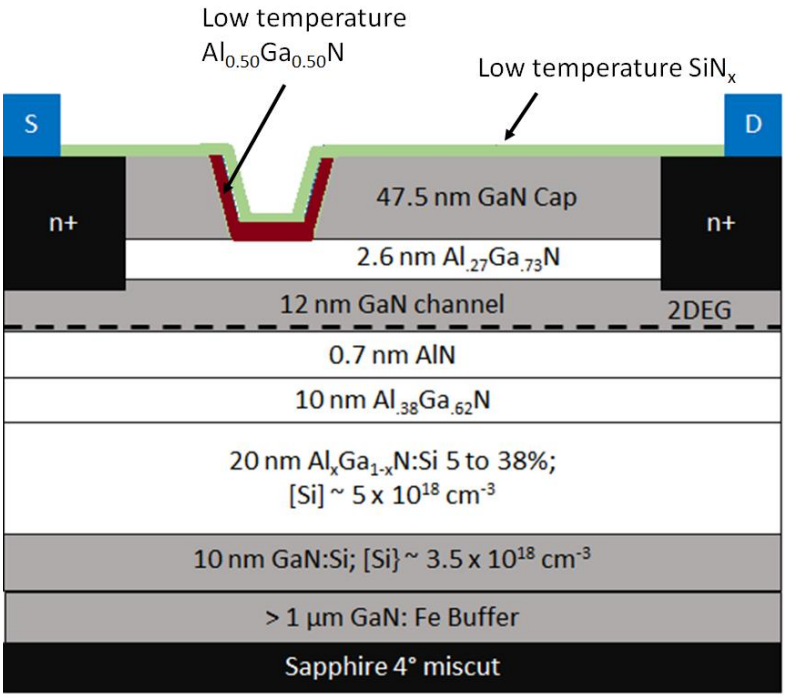

Figure 5.2: The proposed idea is to grow a thin (2 – 3 nm) high Al composition AlGaN in the gate trench followed by a conformal growth of SiN_x.

5.1 Conformal Low Temperature AlGaN and SiNx

For achieving this, we first optimized the conformal regrowth of LT $Al_{0.5}Ga_{0.5}N$ and SiN_x in trenches. Two different temperatures were attempted – 960 and 910 °C (FIB cross-sectional images in figures 5.3 and 5.4 respectively). The trenches were etched on GaN on

sapphire templates. From the cross-sectional images, it was seen that the growth rates on the side-walls vs. the normal direction was more similar for the lower regrowth temperature, i.e. 910 °C, leading to better conformality.

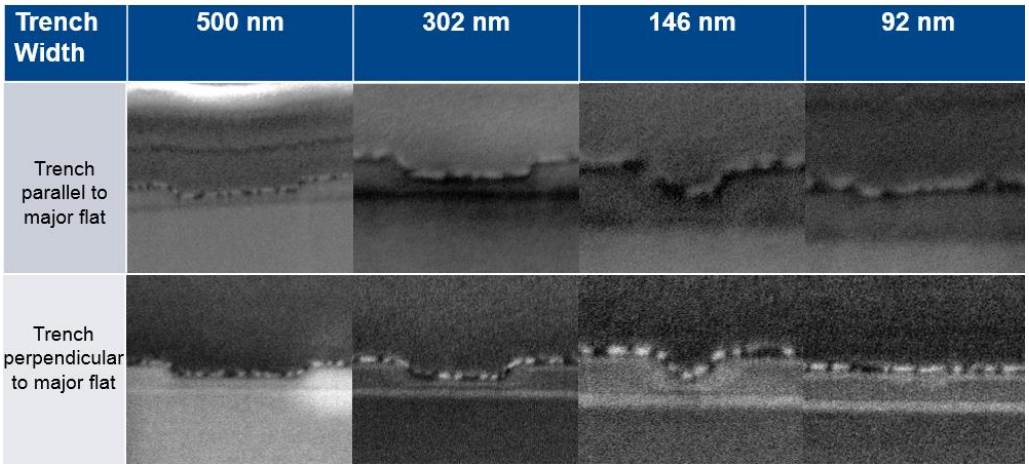

Figure 5.3: FIB cross-sectional images for $Al_{0.5}Ga_{0.5}N$ + SiNx regrowth at 960 °C.

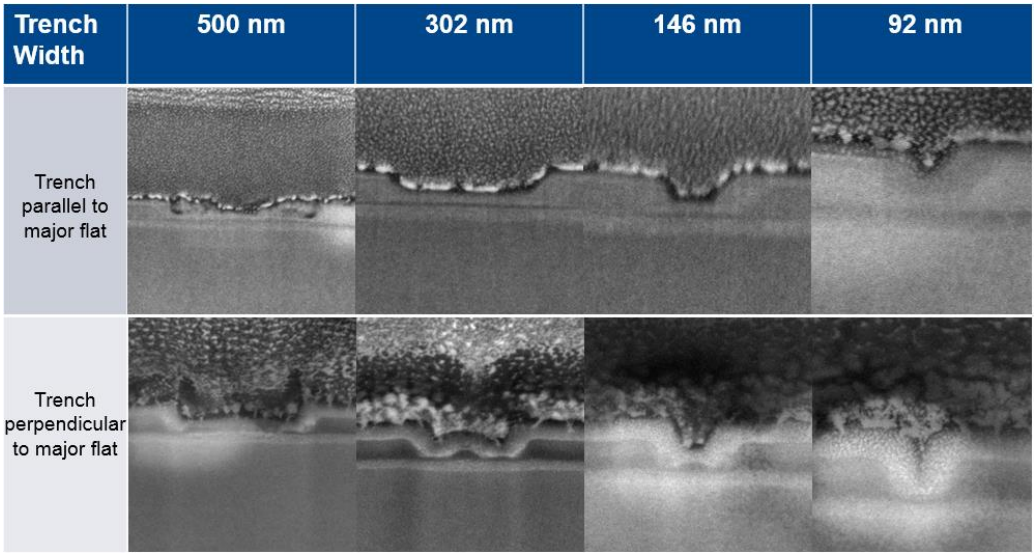

Figure 5.4: FIB cross-sectional images for $Al_{0.5}Ga_{0.5}N$ + SiNx regrowth at 910 °C.

5.2 Channel Charge and Mobility

The SiN_x growth rate was then calibrated at 910 °C in the Thomas Swan reactor (normally grown at 1030 °C) and was measured using an ellipsometer. It was found to be approximately 0.695 Å/s. Then, the entire planar HEMT structure was grown with the new LT $Al_{0.5}Ga_{0.5}N$ and SiN_x layers to ensure that there was little to no impact on channel charge and mobility. The structure for this HEMT is given in figure 5.5. The channel sheet charge was measured via Van der Pauw Hall to be 9.4 x 10^{12} cm^{-2} and the mobility was 1140 cm^2/V-s.

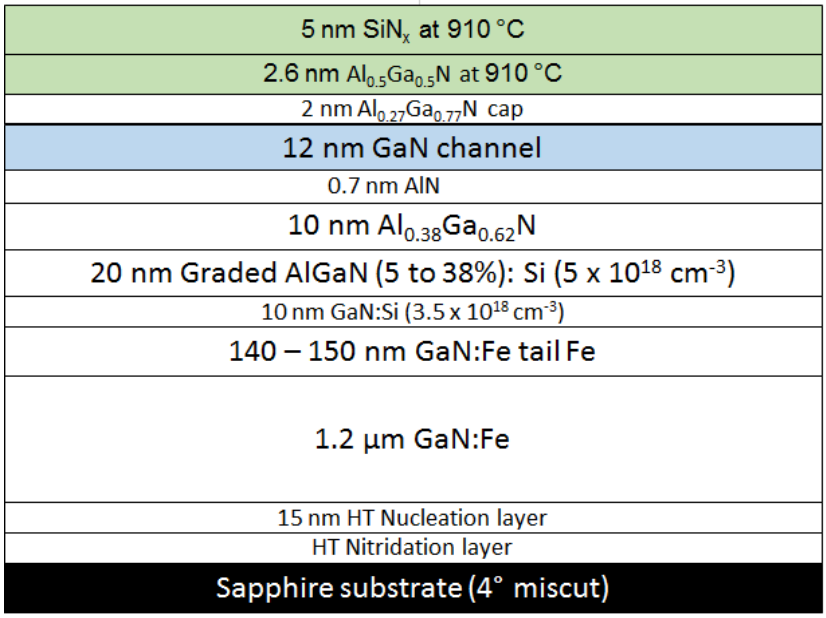

Figure 5.5: Structure of the planar N-polar HEMT with the additional LT (910 °C) $Al_{0.5}Ga_{0.5}N$ + SiNx layers.

5.3 Breakdown Studies

The next step was to perform breakdown measurements on processed HEMTs.[7] A typical N-Polar deep recess epitaxial structure with an AlGaN back-barrier, GaN channel (12 nm), AlGaN cap (2 nm), GaN cap (50 nm) and SiN_x (5 nm) was grown by MOCVD. Simulating a deep recess fabrication process, the SiN_x and GaN cap were plasma etched followed by $Al_{0.50}Ga_{0.50}N$ (2.6 nm)/SiN_x (5 nm) regrowth (Sample A). To characterize the impact of regrowth without etch damage, a sample was grown without GaN cap where the SiN_x was wet etched followed by $Al_{0.50}Ga_{0.50}N$ (2.6 nm)/SiN_x (5 nm) regrowth (Sample B). Finally, a reference in-situ sample was grown with an additional $Al_{0.50}Ga_{0.50}N$ cap (Sample C). The structures for all three samples is given in figure 5.6.

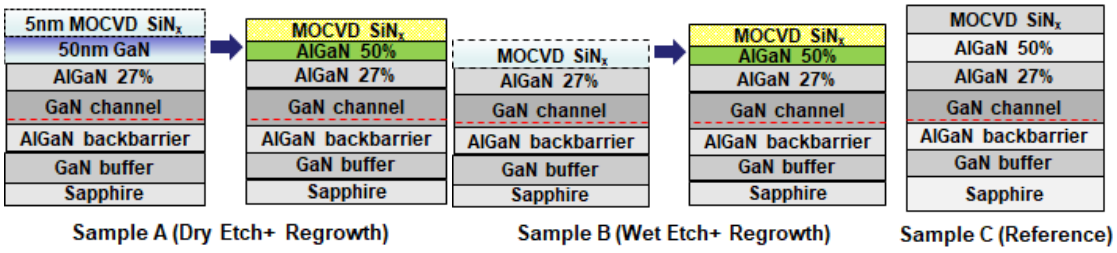

Fig. 5.6. Three samples: A, B & C were chosen to compare the effect of GaN cap etch damage and subsequent AlGaN regrowth on the breakdown voltages of N-polar HEMTs.[7]

Higher charge (1.5×10^{13} vs ~1×10^{13} cm^{-3}) and slightly higher mobility (1300 cm^2/V-s vs 1150 cm^2/V-s) resulted in a relatively higher current density (1 A/mm vs 0.85 A/mm, L_G = 0.75 µm, L_{SD} = 2.5 µm) and lower pinch-off voltage (-7 V vs -5 V) for regrown samples compared to the in-situ reference sample. No dispersion was observed in all three samples.

Both the transfer I-V and 3-terminal breakdown measurements revealed a higher gate-leakage current and a lower V_{BR} for regrown samples compared to the in-situ sample. The in-situ reference sample C demonstrated high breakdown > 100 V (defined at I_D = 1 mA/mm), while introduction of regrowth without dry etch in sample B, lowered the V_{BR} to 48 V. Further lowering of the V_{BR} to 29 V was observed with dry etching in sample A. These results (figure 5.7) indicate that further optimization of the high Al composition AlGaN regrowth is required to emulate the breakdown performance of the in-situ AlGaN cap sample.

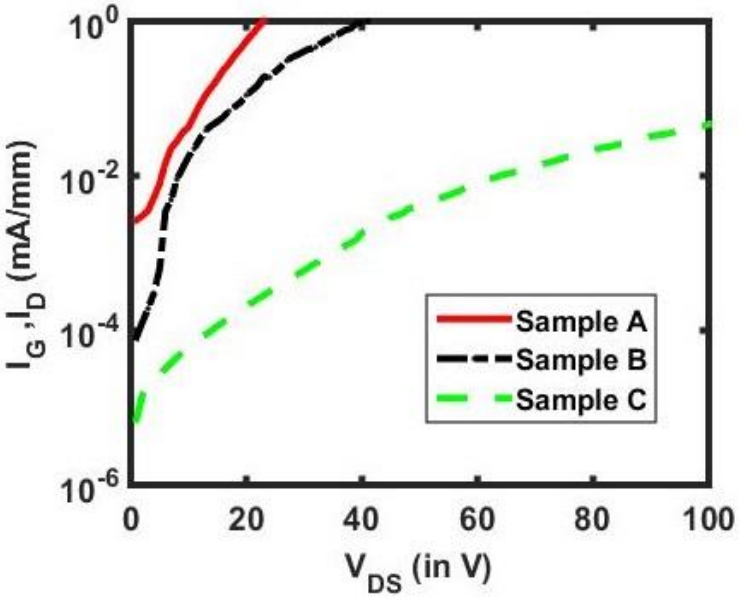

Figure 5.7: 3-terminal breakdown measurements for samples A, B and C indicate that the in-situ grown sample has a significantly higher V_{BR}.[7]

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6 Appendix A

List of some important recipes on MOCVD 4 (Thomas Swan)

Growths and Anneals (on sapphire)

140402GA	Ga-face template
150520GA	Ga-face MESFET on sapphire for Hall measurements with thick n- layers and slow growth rates. The disilane tank was replaced with a low concentration disilane tank. Doping of 1.24 x 10^{18} cm^{-3} and mobility of 350 $cm^2V^{-1}s^{-1}$
150521GA	Ga-face MESFET on sapphire for Hall measurements. Doping of 1.24 x 10^{17} cm^{-3} and mobility of 713 $cm^2V^{-1}s^{-1}$
150527GB	Ga-face MESFET on sapphire for Hall measurements. Doping of 2.75 x 10^{16} cm^{-3} and mobility of 899 $cm^2V^{-1}s^{-1}$
150615GA	Ga-face MESFET on sapphire for Hall measurements. Doping of 1.01 x 10^{16} cm^{-3} and mobility of 899 $cm^2V^{-1}s^{-1}$
150707GA	Ga-face MESFET on sapphire for Hall measurements. Doping of 5.12 x 10^{15} cm^{-3} and mobility of 558 $cm^2V^{-1}s^{-1}$
150615GB	200 nm n+ GaN/6 µm, 1 x 10^{16} cm^{-3} n- GaN/2 µm n+ GaN/ sapphire for diodes

150923GA	3 µm, 1 x 10^{16} cm^{-3} n- GaN drift layer/ n+ GaN, 2 µm, 2.6 x 10^{18} buffer layer/ Sapphire
150807SA	Anneal for 10 mins at 700 °C
150807SB	Anneal for 10 mins at 900 °C
150807SC	Anneal for 10 mins at 800 °C

Regrowths (on GaN or sapphire)

140814SA	5 nm SiN_x regrowth
150603GA	3.3 µm 3.6 x 10^{16} cm^{-3} n- drift layer/ 1 µm 2 x 10^{18} cm^{-3} n+ buffer/ Bulk GaN substrate. Intended for the fabrication of p-n diodes.
150611GA	Ga-face MESFET on bulk GaN for Hall measurements. Doping of 1 x 10^{17} cm^{-3}, n- thickness 2 µm, and mobility of 772 $cm^2V^{-1}s^{-1}$
151125GX	Flow Modulation Epitaxy: 10 nm, 38 loops, 3 seconds rest time between cycles, 675 °C, 2 L NH_3, n-GaN regerowth
151210SIMS	Sample with different Si doping levels and temperatures etc. for SIMS measurements. Regrown on both, bulk GaN and GaN-on-sapphire substrates.
160209SFA	Regrowth of GaN/AlGaN HEMT following activation anneal for Si at 1280 °C. For a CAVET structure.
160209SDB	Regrowth of 30 nm SiN_x after activation anneal for Si at 1280 °C
170615GX	Masked AlN trench filling experiment for Prasad Iyer (Schuller Group)

171103AX	Trench regrowth of Low temperature AlGaN and SiN_x to check for conformality
180313SA	74.7 nm SiNx regrown at 910 °C for calibration (thickness measured from ellipsometer)

List of some important recipes on MOCVD 5 (Nippon Sanso)

Growths (on sapphire)

160928bN	N-polar template
161108as	7 x 10^{17} cm^{-3} doping calibration: 1 µm 7 x 10^{17} cm^{-3} doped GaN / 2 µm u.i.d GaN:Mg / sapphire
170418ds	AlGaN 25%, 20 nm thick calibration layers on bare sapphire

Regrowths (on GaN or sapphire)

160824ap	250 nm p-GaN:Mg regrowth
160918ab	3 µm 8 x 10^{15} cm^{-3} n- GaN/ Bulk GaN for CV doping test
160928ar	3 µm 8 x 10^{15} cm^{-3} n- GaN/ GaN on sapphire for CV doping test
161020cb	PN diode on bulk GaN: 15 nm p++ / 350 nm p / 8 µm n- / 2 µm n+ / Bulk GaN
161108bb	30 nm 10% InGaN calibration grown at 1.05Å/s
161108dp	p-GaN:Mg Interlayer growth 10 nm thick, Mg preflow 15 secs

170419afme	250 nm GaN @ 900 °C / 40 nm u.i.d FME GaN at 660 °C / 300 nm p-GaN / 300 nm HT GaN / S.I. template on sapphire
170419fr	AlGaN 25% 25 nm calibration regrowth on a S.I. template
170609bn	200 nm n+ GaN regrowth
170908cb	300 nm n+ GaN, 5 x 10^{18} - 1 x 10^{19} cm^{-3} / 8 µm n- GaN (1e16) / 2 µm n+ GaN/ bulk GaN